PCI/PCIe/PXI-62010/62006/62005

4-CH, Simultaneous, High Performance Multi-Function Data Acquisition Card
User's Manual

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Advance Technologies; Automate the World.

Using this manual

1.1 Copyright

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1.2 Audience and scope

This manual guides you when using JYTEK multi-function PCI/PCIe/PXI-62010/62006/62005 card. The card's hardware, signal connections, and calibration information are provided for faster application building. This manual is intended for computer programmers and hardware engineers with advanced knowledge of data acquisition and high-level programming.

1.3 How this manual is organized

This manual is organized as follows:

Chapter 1 Introduction: This chapter intoduces the PCI/PCIe/PXI-62010/62006/62005 card including its features, specifications and software support information.

Chapter 2 Installation: This chapter presents the card's layout, package contents, and installation.

Chapter 3 Signal Connections: This part describes the PCI/PCIe/PXI-62010/62006/62005 card signal connections.

Chapter 4 Operation Theory: The operation theory of the PCI/PCIe/PXI-62010/62006/62005 card functions including A/D conversion, D/A conversion, and programmable function I/O are discussed in this chapter.

Chapter 5 Calibration: The chapter offers information on how to calibrate the PCI/PCIe/PXI-62010/62006/62005 card for accurate data acquisition and output.

Warranty Policy: This presents the JYTEK Warranty Policy terms and coverages.

Getting Service: Contact information for JYTEK's worldwide offices.

1.4   Conventions

Take note of the following conventions used throughout the manual to make sure that you perform certain tasks and instructions properly.

NOTE	Additional information, aids, and tips that help you perform particular tasks.

IMPORTANT	Critical information and instructions that you MUST perform to complete a task.

WARNING	Information that prevents physical injury, data loss, module damage, program corruption etc. when trying to complete a particular task.

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JYTEK

1 Introduction

The PCI/PCIe/PXI-62010/62006/62005 card is an advanced data acquisition card based on the 32-bit PCI or PCI Express® architecture. High performance designs and state-of-the-art technology make these cards ideal for data logging and signal analysis applications in medical, process control, etc.

1.1 Features

The PCI/PCIe/PXI-62010/62006/62005 advanced data acquisition card has the following features:

- ▶ 32-bit PCI bus (PCI/PXI models) or PCI Express (PCIe model), plug and play
- ▶ 4-channel simultaneous differential analog input:
  - ▷ PCI/PCIe/PXI-62010: 14-bit Analog input resolution with sampling rate up to 2 MS/s
  - ▷ PCI/PCIe/PXI-62005: 16-bit Analog input resolution with sampling rate up to 500 KS/s
  - ▷ PCI/PCIe/PXI-62006: 16-bit Analog input resolution with sampling rate up to 250 KS/s
- ▶ Programmable bipolar/unipolar analog input
- ▶ Programmable gain (x1, x2, x4, x8 for all PCI-620XX)
- ▶ A/D FIFO
  - ▷ PCI/PCIe/PXI-62010: Total 8 K samples
  - ▷ PCI/PCIe/PXI-62005/62006: Total 512 samples
- ▶ Versatile trigger sources: software trigger, external digital trigger, analog trigger and trigger from System Synchronization Interface (SSI).
- ▶ A/D Data transfer: software polling & bus-mastering DMA with Scatter/Gather functionality
- ▶ Four A/D trigger modes: post-trigger, delay-trigger, pre-trigger and middle-trigger
- ▶ Two-channel DA outputs with waveform generation capability
- ▶ 2 K samples output data FIFO for DA channels
- ▶ DA Data transfer: software update and bus-mastering DMA with Scatter/Gather functionality
- ▶ System Synchronization Interface (SSI)
- ▶ Full A/D/DA auto-calibration
- ▶ Completely jumper-less and software-configurable

1.2 Applications

▶ Automotive Testing

▶ Cable Testing

▶ Transient signal measurement

▶ ATE

▶ Laboratory Automation

▶ Biotech measurement

1.3 Specifications

Analog Input (AI)

▶ Number of channels: 4 differential

▶ A/D converter:
  ▷ PCI/PCIe/PXI-62010: LTC1414 or equivalent
  ▷ PCI/PCIe/PXI-62005: A/D7665 or equivalent
  ▷ PCI/PCIe/PXI-62006: A/D7663 or equivalent

▶ Max sampling rate:
  ▷ PCI/PCIe/PXI-62010: 2MS/s
  ▷ PCI/PCIe/PXI-62005: 500kS/s
  ▷ PCI/PCIe/PXI-62006: 250kS/s

▶ Resolution:
  ▷ PCI/PCIe/PXI-62010: 14 bits, no missing code
  ▷ PCI/PCIe/PXI-62005/62006: 16 bits, no missing code

▶ FIFO buffer size:
  ▷ PCI/PCIe/PXI-62010: 8K samples
  ▷ PCI/PCIe/PXI-62005/62006: 512 samples

▶ Programmable input range:
  ▷ Bipolar: $\pm$10V, $\pm$5V, $\pm$2.5V, $\pm$1.25V
  ▷ Unipolar: 0~10V, 0~5V, 0~2.5V, 0~1.25V

▶ Operational common mode voltage range: $\pm$11V

▶ Overvoltage protection:
  ▷ Power on: continuous $\pm$30V
  ▷ Power off: continuous $\pm$15V

▶ Input impedance: 1GΩ/100pF

► -3dB small signal bandwidth: (Typical, 25°C)

Device	Input Range	Bandwidth (-3dB)	Input Range	Bandwidth (-3dB)
62010	±10V	1170 kHz	0~10V	1090 kHz
	±5V	1050 kHz	0~5V	1020 kHz
	±2.5V	800 kHz	0~2.5V	790 kHz
	±1.25V	530 kHz	0~1.25V	530 kHz
62005	±10V	1160 kHz	0~10V	1210 kHz
	±5V	1050 kHz	0~5V	1050 kHz
	±2.5V	780 kHz	0~2.5V	770 kHz
	±1.25V	520 kHz	0~1.25V	530 kHz
62006	±10V	630 kHz	0~10V	640 kHz
	±5V	620 kHz	0~5V	620 kHz
	±2.5V	540 kHz	0~2.5V	540 kHz
	±1.25V	410 kHz	0~1.25V	420 kHz

Table 1-1: -3dB Small Signal Bandwidth

► Large signal bandwidth (1% THD): 300 kHz

► System Noise: (Typical)

Device	Input Range	System noise	Input Range	System noise
62010	±10V	0.6 LSBrms	0~10V	0.8 LSBrms
	±5V	0.6 LSBrms	0~5V	0.8 LSBrms
	±2.5V	0.6 LSBrms	0~2.5V	0.9 LSBrms
	±1.25V	0.6 LSBrms	0~1.25V	0.9 LSBrms
62005	±10V	1.2 LSBrms	0~10V	1.9 LSBrms
	±5V	1.2 LSBrms	0~5V	2.0 LSBrms
	±2.5V	1.3 LSBrms	0~2.5V	2.1 LSBrms
	±1.25V	1.3 LSBrms	0~1.25V	2.2 LSBrms
62006	±10V	1.0 LSBrms	0~10V	1.5 LSBrms
	±5V	1.0 LSBrms	0~5V	1.6 LSBrms
	±2.5V	1.1 LSBrms	0~2.5V	1.7 LSBrms
	±1.25V	1.1 LSBrms	0~1.25V	1.8 LSBrms

Table 1-2: System Noise

▶ CMRR: (DC to 60 Hz, Typical)

Device	Input Range	CMRR	Input Range	CMRR
62010	±10V	90 dB	0~10V	89 dB
	±5V	92 dB	0~5V	92 dB
	±2.5V	95 dB	0~2.5V	94 dB
	±1.25V	97 dB	0~1.25V	97 dB
62005	±10V	86 dB	0~10V	85 dB
	±5V	88 dB	0~5V	88 dB
	±2.5V	91 dB	0~2.5V	90 dB
	±1.25V	93 dB	0~1.25V	93 dB
62006	±10V	87 dB	0~10V	86 dB
	±5V	89 dB	0~5V	88 dB
	±2.5V	91 dB	0~2.5V	91 dB
	±1.25V	93 dB	0~1.25V	93 dB

Table 1-3: CMRR: (DC to 60 Hz)

▶ Time-base source:
  ▷ Internal 40MHz or External clock Input (fmax: 40 MHz, fmin: 1 MHz, 50% duty cycle)
▶ Trigger modes:
  ▷ Post-trigger, Delay-trigger, Pre-trigger and Middle-trigger
▶ Data transfers:
  ▷ Programmed I/O, and bus-mastering DMA with scatter/gather
▶ Input coupling: DC
▶ Offset error:
  ▷ Before calibration: ±60mV max
  ▷ After calibration: ±1mV max

► Gain error:
  ▷ Before calibration: ±0.6% of output max
  ▷ After calibration: ±0.1% of output max for PCI/PCIe/PXI-62010, ±0.03% of output max for PCI/PCIe/PXI-62005/62006

Analog Output (AO)

▶ Number of channels: Two-channel voltage output

▶ DA converter: LTC7545 or equivalent

▶ Max update rate: 1 MS/s

▶ Resolution: 12 bits

▶ FIFO buffer size:

   ▷ 1k samples per channel when both channels are enabled for timed DA output

   ▷ 2k samples when only one channel is used for timed DA output

▶ Data transfers:

   ▷ Programmed I/O

   ▷ Bus-mastering DMA with scatter/gather

▶ Output range:

   ▷ Bipolar: ±10V or ±AOEXTREF

   ▷ Unipolar: 0~10V or 0~AOEXTREF

▶ Settling time: 3μS to 0.5 LSB accuracy

▶ Slew rate: 20V/μS

▶ Output coupling: DC

▶ Protection: Short-circuit to ground

▶ Output impedance: 0.3Ω typical

▶ Output driving current: ±5mA max.

▶ Stability: Any passive load, up to 1500pF

▶ Power-on state: 0V steady-state

▶ Power-on glitch: ±1.5V/500uS

▶ Relative accuracy:

   ▷ ±0.5 LSB typical, ±1 LSB max

▶ DNL:

   ▷ ±0.5 LSB typical, ±1.2 LSB max

▶ Offset error:

   ▷ Before calibration: ±80mV max

   ▷ After calibration: ±1mV max

- ► Gain error:
  - ▷ Before calibration: ±0.8% of output max
  - ▷ After calibration: ±0.02% of output max
- ► General Purpose Digital I/O (G.P. DIO, 82C55A)
- ► Number of channels: 24 programmable input/output
- ► Compatibility: TTL/CMOS
- ► Input voltage:
  - ▷ Logic Low: VIL=0.8V max; IIL=0.2mA max
  - ▷ High: VIH=2.0V max; IIH=0.02mA max
- ► Output voltage:
  - ▷ Low: VOL=0.5V max; IOL=8mA max
  - ▷ High: VOH=2.7V min; IOH=400 μA
- ► Synchronous Digital Inputs (SDI, for PCI/PCIe/PXI-62010 only)
- ► Number of channels: 8 digital inputs sampled simultaneously with the analog signal input
- ► Compatibility: TTL/CMOS
- ► Input voltage:
  - ▷ Logic Low: VIL=0.8V max; IIL=0.2mA max
  - ▷ Logic High: VIH=2.7V min; IIL=0.02mA max

General Purpose Timer/Counter (GPTC)

- ► Number of channel: 2 up/down timer/counters
- ► Resolution: 16 bits
- ► Compatibility: TTL
- ► Clock source: Internal or external
- ► Max source frequency: 10 MHz

Analog Trigger (A.Trig)

▶ Source:
  ▷ All analog input channels
  ▷ External analog trigger (EXTATRIG)
▶ Level: ±Full-scale, internal; ±10 V external
▶ Resolution: 8 bits
▶ Slope: Positive or negative (software-selectable)
▶ Hysteresis: Programmable
▶ Bandwidth: 400 kHz

External Analog Trigger Input (EXTATRIG)

▶ Input Impedance:
  ▷ 40 kΩ for PCI/PCIe/PXI-62010
  ▷ 2 kΩ for PCI/PCIe/PXI-62005/62006
▶ Coupling: DC
▶ Protection: Continuous ±35 V maximum

Digital Trigger (D.Trig)

▶ Compatibility: TTL/CMOS
▶ Response: Rising or falling edge
▶ Pulse Width: 10 ns min

System Synchronous Interface (SSI)

▶ Trigger lines: 7

Stability

▶ Recommended warm-up time: 15 minutes
▶ On-board calibration reference:
  ▷ Level: 5.000 V
  ▷ Temperature coefficient: ±2 ppm/$^{\circ}$C
  ▷ Long-term stability: 6 ppm/1000 Hr

Physical

▶ Dimensions:

    ▷ 175mm by 107mm for PCI/PCIe62010/62000

    ▷ Standard CompactPCI form factor for PXI-62010/62000

▶ I/O connector: 68-pin female VHDCI type (e.g. AMP-787254-1)

Power Requirement (typical)

▶ +5VDC

    ▷ 1.82 A for PCI/PXI-62010

    ▷ 2.04 A for PCI/PXI-62005

    ▷ 1.82 A for PCI/PXI-62006

▶ +12 VDC

    ▷ 550 mA for PCIe-62005

    ▷ 460 mA for PCIe-62006

    ▷ 448 mA for PCIe-62010

▶ +3.3 VDC

    ▷ 1.02 A for PCIe-62005

    ▷ 1.02 A for PCIe-62005

    ▷ 1.25 A for PCIe-62010

Operating Environment

▶ Ambient temperature: 0°C to 55°C

▶ Relative humidity: 10% to 90% non-condensing

Storage Environment

▶ Ambient temperature: -20°C to 80°C

▶ Relative humidity: 5% to 95% non-condensing

Interface Connector

▶ 68-pin AMP-787254-1 or equivalent

1.4 Software Support

JYTEK provides versatile software drivers and packages for users' different approach to building up a system. JYTEK not only provides programming libraries such as DLL for most Windows-based systems, but also provide other drivers. All software drivers are included in JYTEK All-in-One USB Flash Driver. Contact your JYTEK to get the free SeeSharp® open source software.

Programming Library

For customers who are writing their own programs, we provide function libraries for many different operating systems, including:

D2K-DASK: Include device drivers and DLL for Windows® 7/10. DLL is binary compatible across Windows 7/10. This means all applications developed with D2K-DASK are compatible across Windows 7/10. The developing environment can be VB, VC++, Delphi, BC5, or any Windows programming language that allows calls to a DLL. The user's guide and function reference manual of D2K-DASK are on the website. (www.jytek.com)

D2K-DASK/X: Include device drivers and shared library for Linux. The developing environment can be Gnu C/C++ or any programming language that allows linking to a shared library. The user's guide and function reference manual of D2K-DASK/X are on the website. (www.jytek.com)

2   Installation

This chapter describes how to install the PCI/PCIe/PXI-62010/62006/62005 card. The contents of the package and unpacking information that you should be aware of are outlined first.

The PCI/PCIe/PXI-62010/62006/62005 card performs an automatic configuration of the IRQ and port address. You can use the PCI_SCAN software utility to read the system configuration.

2.1   Contents of Package

In addition to this User's Manual, the package includes the following items:

▶ PCI/PCIe/PXI-62010/62006/62005 multi-function data acquisition card

If any of these items are missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.

2.2   Unpacking

Your PCI/PCIe/PXI-62010/62006/62005 card contains electro-static sensitive components that can be easily be damaged by static electricity.

Therefore, the card should be handled on a grounded anti-static mat. The operator should be wearing an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the card package for obvious damages. Shipping and handling may cause damage to the card. Be sure there are no shipping and handling damages on the modules carton before continuing.

After opening the card module carton, extract the system module and place it only on a grounded anti-static surface with component side up.

Again, inspect the module for damages. Press down on all the socketed IC's to make sure that they are properly seated. Do this only with the module place on a firm flat surface.

You are now ready to install your PCI/PCIe/PXI-62010/62006/62005 card.

NOTE   DO NOT APPLY POWER TO THE CARD IF IT HAS BEEN DAM-

2.3 Card Layout

PCIe-62010/62006/62005

Board to Board Connector

68-Pin Connector

Daughter Board

Carrier Board

Board to Board Connector
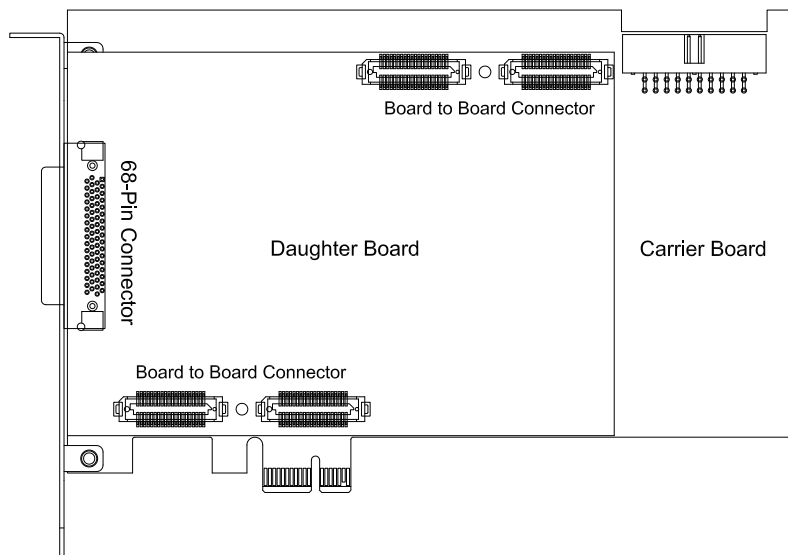
Figure 2-1: PCIe-62010/62006/62005 Card Layout

PCI-62010/62006/62005
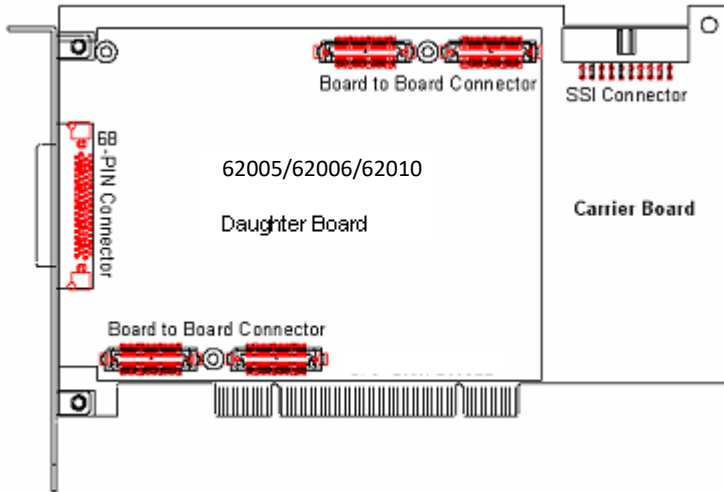
Figure 2-2: PCI-62010/62006/62005 Card Layout

PXI-62010/62006/62005
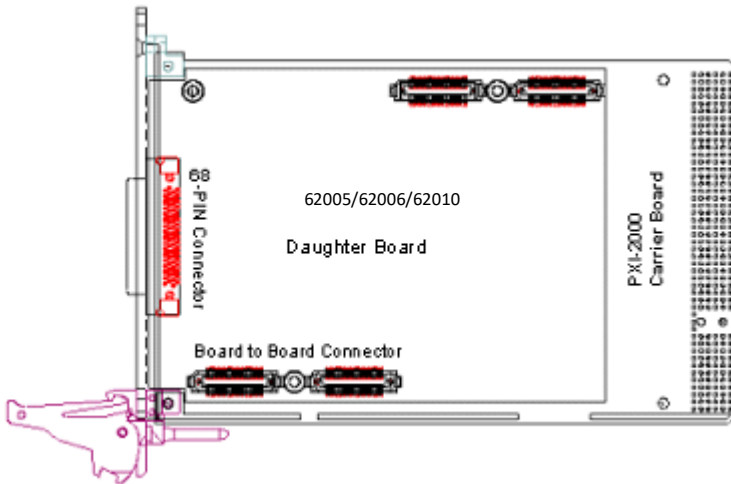
Figure 2-3: PXI-62010/62006/62005 Card Layout

2.4   PCI Configuration

Plug and Play

With support for plug and play, the card requests an interrupt number via its PCI controller. The system BIOS responds with an interrupt assignment based on the card information and on known system parameters. These system parameters are determined by the installed drivers and the hardware load seen by the system.

Configuration

The board configuration is done on a board-by-board basis for all PCI boards in the system. Because configuration is controlled by the system and software, there is no jumper setting required for base address, DMA, and interrupt IRQ.

The configuration is subject to change with every boot of the sys-tem as new boards are added or removed.

Troubleshooting

If your system doesn't boot or if you experience erratic operation with your PCI board in place, it is likely caused by an interrupt con-flict. The BIOS Setup may be incorrectly configured. Consult the BIOS documentation that comes with your system to solve this problem.

3 Signal Connections

This chapter describes PCI/PCIe/PXI-62010/62006/62005 card connectors and the signal connection between the PCI/PCIe/PXI-62010/62006/62005 card and external devices.

3.1 Connectors Pin Assignment

The PCIe/PXI-62010/62006/62005 card is equipped with one 68-pin VHDCI-type connector (AMP-787254-1). It is used for digital input/output, analog input/output, timer/counter signals, etc. One 20-pin ribbon male connector is used for SSI (System Synchronous Interface) in PCI-62010/62006/62005 card. The pin assignments of the connectors are defined in Table 3-1 and Table 3-2.

VHDCI-type (68-pin) Connector

CH0+	1	35	CH0-
CH1+	2	36	CH1-
CH2+	3	37	CH2-
CH3+	4	38	CH3-
EXTATRIG	5	39	AIGND
DA1OUT	6	40	AOGND
DA0OUT	7	41	AOGND
AOEXTREF	8	42	AOGND
SDI3_1 / NC*	9	43	SDI3_0 / NC*
SDI2_1 / NC*	10	44	SDI2_0 / NC*
SDI1_1 / NC*	11	45	SDI1_0 / NC*
SDI0_1 / NC*	12	46	SDI0_0 / NC*
AO_TRIG_OUT	13	47	EXTWFTRG
AI_TRIG_OUT	14	48	EXTDTRIG
GPTC1_SRC	15	49	DGND
GPTC0_SRC	16	50	DGND
GPTC0_GATE	17	51	GPTC1_GATE
GPTC0_OUT	18	52	GPTC1_OUT
GPTC0_UPDOWN	19	53	GPTC1_UPDOWN
EXTTIMEBASE	20	54	DGND
AFI1	21	55	AFI0
PB7	22	56	PB6
PB5	23	57	PB4
PB3	24	58	PB2
PB1	25	59	PB0
PC7	26	60	PC6
PC5	27	61	PC4
DGND	28	62	DGND
PC3	29	63	PC2
PC1	30	64	PC0
PA7	31	65	PA6
PA5	32	66	PA4
PA3	33	67	PA2
PA1	34	68	PA0

Table 3-1: VHDCI-type (68-pin) Connector Pin Assignment

*SDI for PCI/PCIe/PXI-62010 only. NC for PCI/PCIe/PXI-62005/62006.

Legend:

Pin #	Signal Name	Reference	Direction	Description
1~4	CH<0..3>+	CH0<0..3>-	Input	Differential positive input for AI channel <0..3>
5	EXTATRIG	AIGND	Input	External AI analog trigger
6	DA0OUT	AOGND	Output	AO channel 0
7	DA1OUT	AOGND	Output	AO channel 1
8	AOEXTREF	AOGND	Input	External reference for AO channels
9~12	SDI<3..0>_1 (62010) NC (62005/62006)	DGND	Input	Synchronous digital inputs
13	AO_TRIG_OUT	DGND	Output	AO trigger signal
14	AI_TRIG_OUT	DGND	Output	AI trigger signal
15,16	GPTC<0,1>_SRC	DGND	Input	Source of GPTC<0,1>
17,51	GPTC<0,1>_GATE	DGND	Input	Gate of GPTC<0,1>
18,52	GPTC<0,1>_OUT	DGND	Input	Output of GPTC<0,1>
19,53	GPTC<0,1>_UPDOWN	DGND	Input	Up/Down of GPTC<0,1>
20	EXTTIMEBASE	DGND	Input	External TIMEBASE
21,28,49, 50,54,62	DGND	--------	--------	Digital ground
22,56,23,5 7,24,58,25 ,59	PB<7,0>	DGND	PIO*	Programmable DIO pins of 8255 Port B
26,60,27,6 1,29,63,3 0,64	PC<7,0>	DGND	PIO*	Programmable DIO pins of 8255 Port C
31,65,32, 66,33,67,3 4,68	PA<7,0>	DGND	PIO*	Programmable DIO pins of 8255 Port A
35~38	CH<0..3>-	--------	Input	Differential negative input for AI channel <0..3>

Table 3-2: VHDCI-type (68-pin) Connector Legend

Pin #	Signal Name	Reference	Direction	Description
39	AIGND	--------	--------	Analog ground for AI
40~42	AOGND	--------	--------	Analog ground for AO
43~46	SDI<3..0>_0 (62010) NC (62005/62006)	DGND	Input	Synchronous digital inputs
47	EXTWFTRIG	DGND	Input	External AO waveform
trigger				
48	EXTDTRIG	DGND	Input	External AI digital trigger
55	AFI0	DGND	Input	Auxiliary Function Input 0 (ADCONV, AD_START)
21	AFI1	DGND	Input	Auxiliary Function Input 1 (DAWR, DA_START)

Table 3-2: VHDCI-type (68-pin) Connector Legend

*PIO means programmable I/O

SSI Connector (J3)

SSI_TIMEBASE	1	2	DGND
SSI_ADCONV	3	4	DGND
SSI_DAWR	5	6	DGND
SSI_SCAN_START	7	8	DGND
RESERVED	9	10	DGND
SSI_AD_TRIG	11	12	DGND
SSI_DA_TRIG	13	14	DGND
RESERVED	15	16	DGND
RESERVED	17	18	DGND
RESERVED	19	20	DGND

Table 3-3: SSI Connector (JP3) Pin Assignment for DAQ Models

Legend:

SSI timing signal	Functionality
SSI_TIMEBASE	SSI master: send the TIMEBASE out SSI slave: accept the SSI_TIMEBASE to replace the internal TIMEBASE signal.
SSI_ADCONV	SSI master: send the ADCONV out SSI slave: accept the SSI_ADCONV to replace the internal ADCONV signal.
SSI_SCAN_START	SSI master: send the SCAN_START out SSI slave: accept the SSI_SCAN_START to replace the internal SCAN_START signal.
SSI_AD_TRIG	SSI master: send the internal AD_TRIG out SSI slave: accept the SSI_AD_TRIG as the digital trigger signal.
SSI_DAWR	SSI master: send the DAWR out. SSI slave: accept the SSI_DAWR to replace the internal DAWR signal.
SSI_DA_TRIG	SSI master: send the DA_TRIG out. SSI slave: accept the SSI_DA_TRIG as the digital trigger signal.

Table 3-4: SSI Connector Legend

3.2　Analog Input Signal Connection

The PCI/PCIe/PXI-62010/62006/62005 card provides 4 differential analog input channels. The analog signal can be converted to digital values by the A/D converter. To avoid ground loops and get more accurate measurements from the A/D conversion, it is quite important to understand the signal source type and how to connect the analog input signals.

Types of signal sources

Ground-Referenced Signal Sources

A ground-referenced signal means it is connected in some way to the building system. That is, the signal source is already connected to a common ground point with respect to the PCI/PCIe/PXI-62010/62006/62005 card, assuming that the computer is plugged into the same power system. Non-isolated out-puts of instruments and devices that plug into the buildings power system are ground-referenced signal sources.

Floating Signal Sources

A floating signal source means it is not connected in any way to the buildings ground system. A device with an isolated output is a floating signal source, such as optical isolator outputs, transformer outputs, and thermocouples.

Single-Ended Measurements

For single-ended connection, the analog input signal is referenced to the common ground of the system. In this case, all the negative ends of analog input channels should be connected to the AIGND on the connector in-stead of floating. Refer to Figure 3-1.
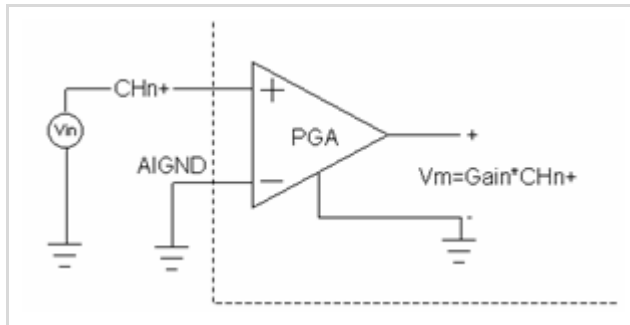
Figure 3-1: Single-Ended Connections

In single-ended configurations, more electrostatic and magnetic noise couples into the single connections than in differential configurations. Therefore, the single-ended connection is not recommended unless minimal wire connections are necessary.

Differential Measurements

Differential Connection for Grounded-Reference Signal Sources

The differential analog input provides two inputs that respond to the signal voltage difference between them. If the signal source is ground-referenced, the differential mode can be used for the common-mode noise rejection. Figure 3-2 shows the connection of ground-referenced signal sources under the differential input mode.
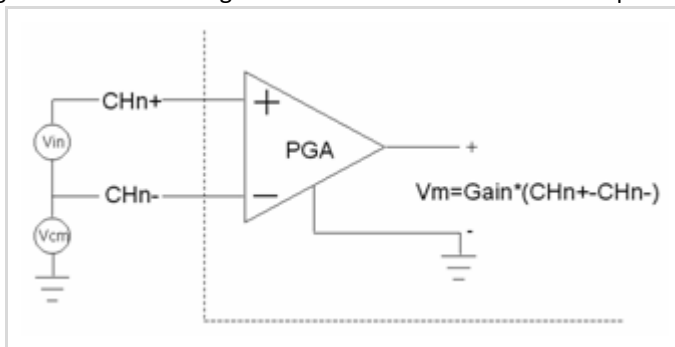

Figure 3-2: Ground-referenced Source and Differential Input

Differential Connection for Floating Signal Sources

Figure 3-3 shows how to connect a floating signal source to PCI/PCIe/PXI-62010/62006/62005 card in differential input mode. For floating signal sources, you need to add a resistor at each channel to provide a bias return path. The resistor value should be about 100 times the equivalent source impedance. If the source impedance is less than 100 ohms, you can simply connect the negative side of the signal to AGND as well as the negative input of the Instrumentation Amplifier, without any resistors at all. In differential input mode, less noise couples into the signal connections than in single-ended mode.
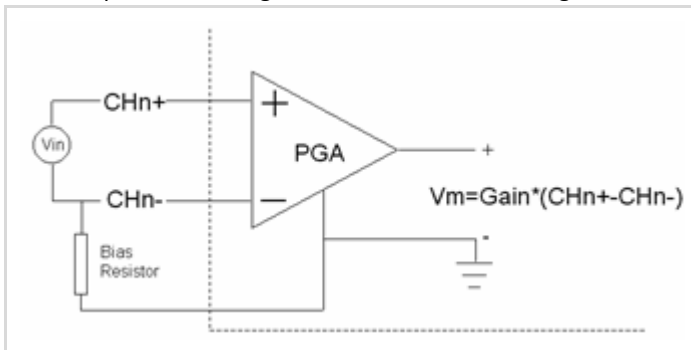

Figure 3-3: Floating Source and Differential Input

4 Operation Theory

The operation theory of the PCI/PCIe/PXI-62010/62006/62005 card functions are described in this chapter. The functions include the A/D conversion, D/A conversion, digital I/O, and general purpose counter/timer. The operation theory can help you understand how to configure and program the PCI/PCIe/PXI-62010/62006/62005 card.

The whole PCI/PCIe/PXI card series, including the PCI/PCIe/PXI-62010/62000 Series, PCI/PCIe/PXI-62200 Series, and PCI/PCIe/PXI-62500 Series, are designed based on the same logic-timing template of PCI/PCIe/PXI-622XX. In the PCI/PXI-622XX cards, all the A/D related timings are for multiplexing A/D sampling based on scanning, so that PCI/PCIe/PXI-62010/62006/62005 card also adopts the same concept, except there is only one conversion signal in a scan which could generate up to four samples from the four different channels at the same time. In the following description, to conform to the original timing design, we still use **scan** as the unit of A/D data acquisition. All the DA and GPTC functions are the same in PCI/PCIe/PXI-62010/62006/62005 card and PCI/PCIe/PXI-62200 Series, while PCI/PCIe/PXI-62500 Series provides improved DA timing compared to the two earlier series.

4.1 A/D Conversion

When using an A/D converter, you must know about the properties of the signal to be measured. You may decide which channel to use and how to connect the signals to the card. In addition, users should define and control the A/D signal configurations, including channels, gains, and polarities (unipolar/bipolar).

The A/D acquisition is initiated by a trigger source and you must decide how to trigger the A/D conversion. The data acquisition will start once a trigger condition is matched.

After the end of an A/D conversion, the A/D data is buffered in a Data FIFO. The A/D data can now be transferred into the system memory for further processing.

PCI/PCIe/PXI-62010 AI Data Format
Synchronous Digital Inputs (PCI/PCIe/PXI-62010 only)

When each A/D conversion is completed, the 14-bits converted digital data accompanied with 2 bits of SDI<1..0>_X per channel from J5 will be latched into the 16-bit register and data FIFO as shown in Figure 4-1 and Figure 4-2. Therefore, you can simultaneously sample one analog signal with four digital signals. The data format of every acquired 16-bit data is as follows:

D13, D12, D11 ……. D1, D0, b1, b0
Where
D13, D12, D11 ……. D1, D0: 2's complement A/D 14-bit data
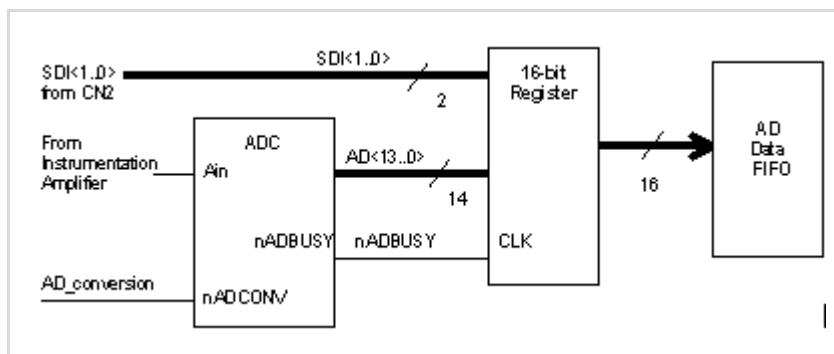b1, b0: Synchronous Digital Inputs SDI<1..0>

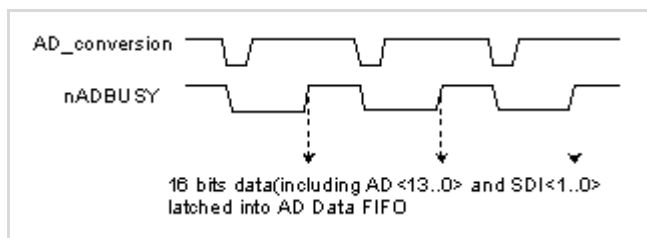**Figure 4-1: Synchronous Digital Inputs Block Diagram**

Figure 4-2: Synchronous Digital Inputs Timing

NOTE	Since the analog signal is sampled when an A/D conversion starts (falling edge of A/D_conversion signal), while SDI<1..0> are sam-pled right after an A/D conversion completes (rising edge of nADBUSY signal). Precisely SDI<1..0> are sampled within 220 to 400ns lag to the analog signal, due to the variation of the conversion time of the A/D converters.

Table 4-1and Table 4-2 illustrate the ideal transfer characteristics of various input ranges of PCI/PCIe/PXI-62000/62010 Series card. The converted digital codes for PCI/PCIe/PXI-62010 are 14-bit and 2's complement, and here we present the codes as hexadecimal numbers. Note that the last 2 bits of the transferred data, which are the synchronous digital input (SDI), should be ignored when retrieving the analog data, and that the last two digital codes are SDI<1..0>)

Description	Bipolar Analog Input Range				Digital code
Full-scale Range	±10V	±5V	±2.5V	±1.25V	
Least significant bit	1.22mV	0.61mV	0.305mV	0.153mV	
FSR-1LSB	9.9988V	4.9994V	2.4997V	1.2499V	1FFF
Midscale +1LSB	1.22mV	0.61mV	0.305mV	0.153mV	0001
Midscale	0V	0V	0V	0V	0000
Midscale −1LSB	-1.22mV	-0.61mV	-0.305mV	-0.153mV	3FFF
-FSR	-10V	-5V	-2.5V	-1.25V	2000

Table 4-1: Bipolar Analog Input Range and Output Digital Code on PCI/PCIe/PXI-62010

Description	Unipolar Analog Input Range				Digital code
Full-scale Range	0V to 10V	0 to +5V	0 to +2.5V	0 to +1.25V	
Least significant bit	0.61mV	0.305mV	0.153mV	76.3uV	
FSR-1LSB	9.9994V	4.9997V	2.9999V	1.2499V	1FFF
Midscale +1LSB	5.00061V	2.50031V	1.25015V	625.08mV	0001
Midscale	5V	2.5V	1.25V	625mV	0000
Midscale −1LSB	4.99939V	2.49970V	1.24985V	624.92mV	3FFF
-FSR	0V	0V	0V	0V	2000

Table 4-2: Unipolar Analog Input Range and Output Digital Code on PCI/PCIe/PXI-62010

PCI/PCIe/PXI-62005/62006 AI Data Format

The data format of the acquired 16-bit A/D data is **binary coding**. Table 4-3 and Table 4-4 illustrate the valid input ranges and the ideal transfer characteristics. The converted digital codes for PCI/PCIe/PXI-62005/62006 are 16-bit and direct binary, and here the codes were presented as hexadecimal numbers.

Description	Bipolar Analog Input Range				Digital code
Full-scale Range	±10V	±5V	±2.5V	±1.25V	
Least significant bit	305.2uV	152.6uV	76.3uV	38.15uV	
FSR-1LSB	9.999695V	4.999847V	2.499924V	1.249962V	FFFF
Midscale +1LSB	305.2uV	152.6uV	76.3uV	38.15uV	8001
Midscale	0V	0V	0V	0V	8000
Midscale -1LSB	-305.2uV	-152.6uV	-76.3uV	-38.15uV	7FFF
-FSR	-10V	-5V	-2.5V	-1.25V	0000

Table 4-3: Bipolar Analog Input Range and Output Digital Code for PCI/PCIe/PXI-62005/62006

Description	Unipolar Analog Input Range				Digital code
Full-scale Range	0V to 10V	0 to +5V	0 to +2.5V	0 to +1.25V	
Least signifi-cant bit	152.6uV	76.3uV	38.15uV	19.07uV	
FSR-1LSB	9.999847V	4.999924V	2.499962V	1.249981V	FFFF
Midscale +1LSB	5.000153V	2.500076V	1.250038V	0.625019V	8001
Midscale	5V	2.5V	1.25V	0.625V	8000
Midscale -1LSB	4.999847V	2.499924V	1.249962V	0.624981V	7FFF
-FSR	0V	0V	0V	0V	0000

Table 4-4: Unipolar Analog Input Range and Output Digital Code for PCI/PCIe/PXI-62005/62006

Software Conversion with Polling Data Transfer Acqui-sition Mode (Software Polling)

This is the easiest way to acquire a single A/D data. The A/D converter starts one conversion whenever the dedicated software command is executed. Then the software would poll the conversion status and read the A/D data back when it is available.

This method is very suitable for applications that needs to process A/D data in real time. Under this mode, the timing of the A/D conversion is fully controlled by the software. However, it is difficult to control the A/D conversion rate.

Specifying Channel, Gain, and Polarity

In both the Software Polling and programmable scan acquisition mode, the channel, gain, and polarity for each channel can be speci-fied and selected. With this configuration, signal sources must be connected to the right connector as the specified settings.

When the specified channels have been sampled from the first to the last data, the settings applied to each channel would be the same until next change.

Example:

Typically you can set the input configuration for different channels:

Ch1 with unipolar ±10V
Ch2 with bipolar ±2.5V
Ch3 with no signal input (disabled)
Ch4 with bipolar ±1.25V

Programmable Scan Acquisition Mode
Scan Timing and Procedure

It's recommended that this mode be used if your applications need a fixed and precise A/D sampling rate. You can accurately program the period between conversions of individual channels. There are at least two counters which need to be specified:

SI_counter (24 bit):Specify the Scan Interval = SI_counter / TIMEBASE
PSC_counter (24 bit):Specify Post Scan Counts, i.e. the total sample count after a trigger event,

The acquisition timing and the meanings of the 2 counters are illustrated in Figure 4-3. The SCAN_START signal is derived from the SI_counter, which will lead to the A/D conversion signal generation. Note that the PCI/PCIe/PXI-62010/62006/62005 card is a simultaneous sampling A/D card, so the **scan interval** equals the **sampling interval**.

Example: Post-trigger acquisition

Set

SI_counter = 160
PSC_counter = 30
TIMEBASE = Internal clock source

Then
Scan Interval = 160/40M s = 4 us
Total acquisition time = 30 X 4 us = 120 us

TIMEBASE Clock Source

In scan acquisition mode, all the A/D conversions start on the output of counters, which use TIMEBASE as the clock source. By software you can specify the TIMEBASE to be either an internal clock source (onboard 40 MHz clock) or an external clock input (EXTTIMEBASE) on J5 connector (68-pin VHDCI). The external TIMEBASE is useful when you want to acquire data at rates not available with the internal A/D sample clock. The external clock source should generate TTL-compatible continuous clocks and with a maximum frequency of 40 MHz while the minimum should be 1 MHz. Refer to section 4.6 for information on user-controllable timing signals.
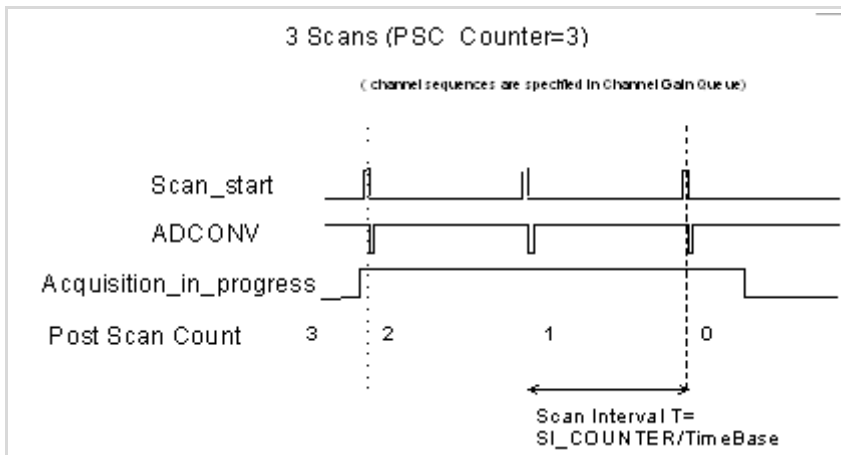
Figure 4-3: Scan Timing

There are four trigger modes to start the scan acquisition. Refer to section 4.1 for details. The data transfer mode is discussed in the following section.

NOTES	The maximum A/D sampling rate is 2 MHz for PCI/PCIe/PXI-62010, 500 kHz for PCI/PCIe/PXI-62005, 250 kHz for PCI/PCIe/PXI-62006. Therefore, the minimum setting of SI_counter is 20 for PCI/PCIe/PXI-62010, 80 for PCI/PCIe/PXI-62005, 160 for PCI/PCIe/PXI-62006 while using the internal TIMEBASE.
	The SI_counter is a 24-bit counter. Therefore, the maximum scan interval while using an internal TIMEBASE = 224/40 Ms = 0.419 s.

Trigger Modes

The PCI/PCIe/PXI-62010/62006/62005 card provides four trigger sources (internal software trigger, external analog trigger, external digital trigger, and SSI trigger signals). You must select one of them as the source of the trigger event. A trigger event occurs when the specified condition is detected on the selected trigger source. For example, a rising edge on the external digital trigger input. Refer to section 4.6 for more information on SSI signals.

There are four trigger modes (pre-trigger, post-trigger, middle-trigger, and delay-trigger) working with the four trigger sources to initiate different scan data acquisition timing when a trigger event occurs. They are described in the following sections. For information on trigger sources, refer to section 4.5.

Pre-Trigger Acquisition

Use pre-trigger acquisition in applications where you want to collect data before a trigger event. The A/D starts to sample when you execute the specified function calls to begin the pre-trigger operation, and it stops when the trigger event occurs. Users must program the value M in M_counter (16 bits) to specify the amount of the stored scans before the trigger event. If an external trigger occurs, the program only stores the last M scans of data converted before the trigger event, as illustrated in Figure 4-4, where M_counter = M =3, PSC_counter = 0. The post scan count is 0 because there is no sampling after the trigger event in pre-trigger acquisition. The total stored amount of data = Number of enabled channels * M_counter.
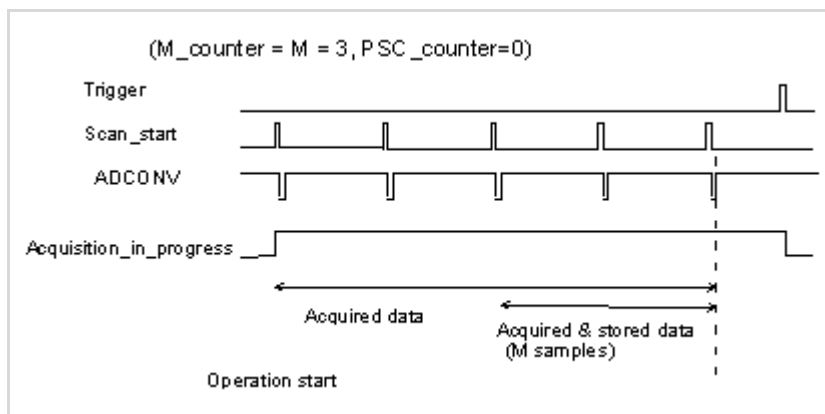
Figure 4-4: Pre-trigger

Note that If the trigger event occurs when a conversion is in progress, the data acquisition will not stop until this conversion is completed and the stored M scans of data include the last scan, as illustrated in Figure 4-5, where M_counter = M = 3, PSC_counter = 0.
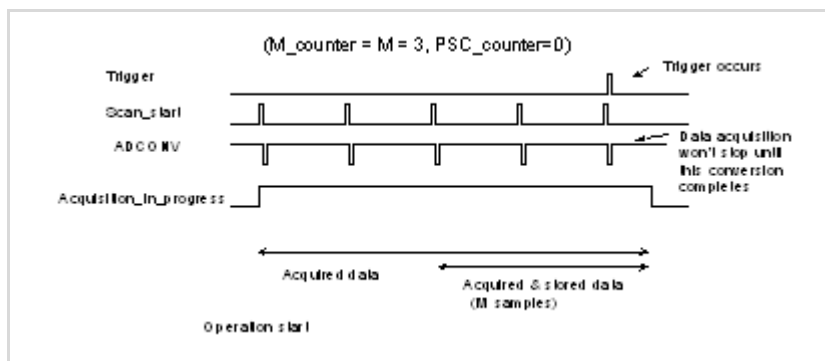

Figure 4-5: Pre-trigger Scan Acquisition

When the trigger signal occurs before the first M scans of data are converted, the amount of stored data could be fewer than the originally specified amount M_counter, as illustrated in Figure 4-6. This situation can be avoided by setting M_enable. If M_enable is set to 1, the trigger signal will be ignored until the first M scans of data are converted, and it assures the user M scans of data under pre-trigger mode, as illustrated in Figure 4-7. However, if M_enable is set to 0, the trigger signal will be accepted any time, as shown in Figure 4-6. Note that the total amount of stored data will always be equal to the number in the M_counter because data acquisition does not stop until a scan is completed.
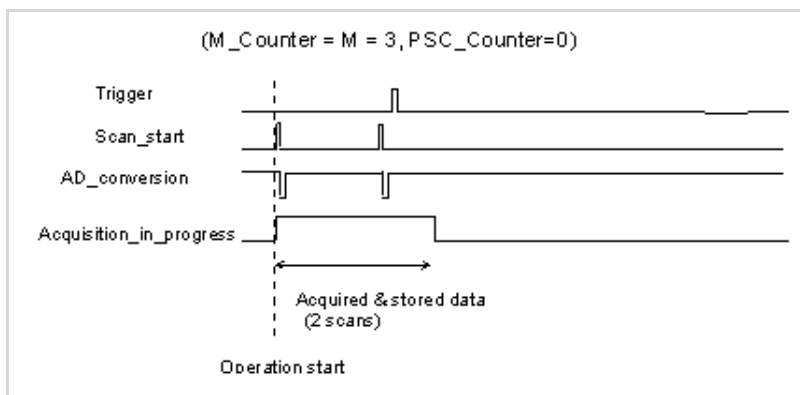

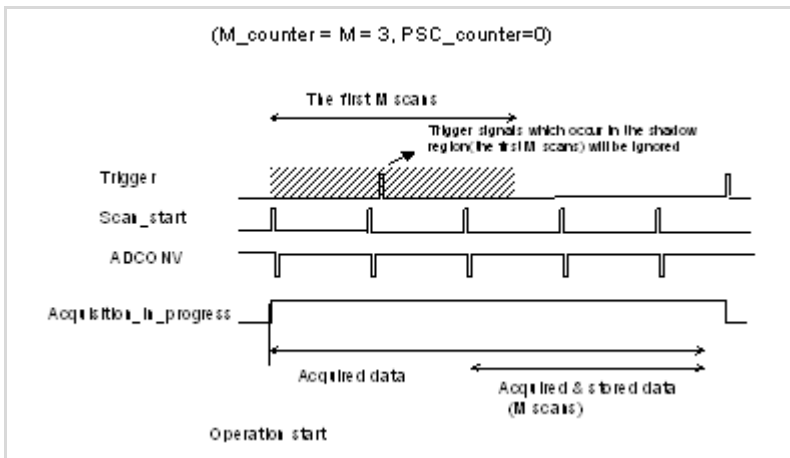**Figure 4-6: Pre-trigger with M_enable=0**

Figure 4-7: Pre-trigger with M_enable=1

NOTE   The PSC_counter is set to 0 in pre-trigger acquisition mode.

Middle-Trigger Acquisition

Use middle-trigger acquisition in applications where you want to collect data before and after a trigger event. The number of scans (M) stored before the trigger is specified in M_counter, while the number of scans (N) after the trigger is specified in PSC_counter.

Like pre-trigger mode, the number of stored data could be less than the specified amount of data (M+N), if an external trigger occurs before M scans of data are converted. The M_enable bit in middle-trigger mode takes the same effect as in pre-trigger mode. If M_enable is set to 1, the trigger signal will be ignored until the first M scans of data are converted, and it assures the user with (M+N) scans of data under middle-trigger mode. However, if M_enable is set to 0, the trigger signal will be accepted at any time. Figure 4-8 shows the acquisition timing with M_enable=1.
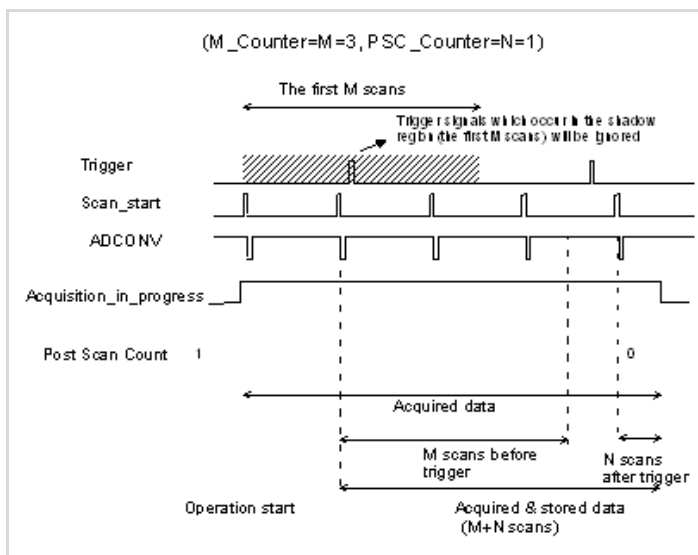
Figure 4-8: Middle-Trigger with M_enable = 1

If the trigger event occurs when a scan is in progress, the stored N scans of data would include this scan, as illustrated in Figure 4-9.
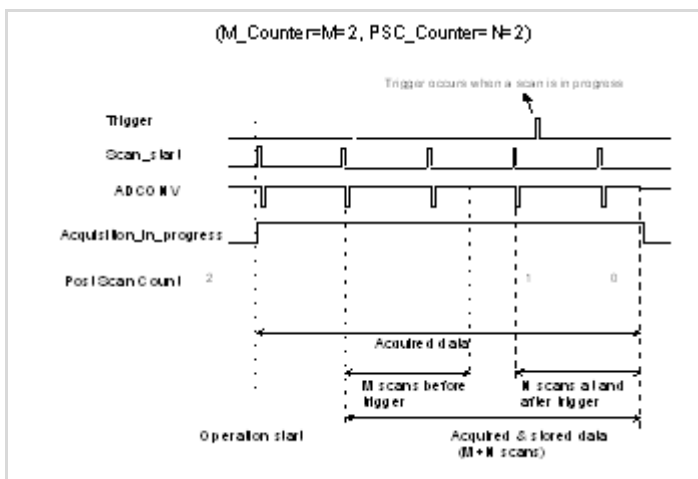

Figure 4-9: Middle-Trigger

NOTE   The M_counter defined in Middle-Trigger is different from that of the Pre-Trigger. In Middle-Trigger, M_Counter ends counting before the trigger event while in Pre-Trigger, M_Counter ends counting right at or before trigger event. Refer to Figure 4-6 and Figure 4-9.

Post-Trigger Acquisition

Use post-trigger acquisition in applications where you want to collect data after a trigger event. The number of scans after the trigger is specified in PSC_counter, as illustrated in Figure 4-10. The total acquired data length = number of enable-channel * PSC_counter.
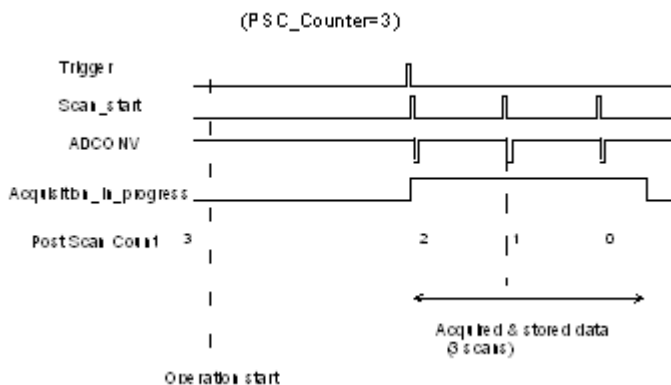

Figure 4-10: Post trigger

Delay Trigger Acquisition

Use delay trigger acquisition in applications where you want to delay the data collection after the occurrence of a specified trigger event. The delay time is controlled by the value, which is pre-loaded in the Delay_counter (16-bit). The counter counts down on the rising edge of the Delay_counter clock source after the trigger condition is met. The clock source can be software-programmed either by the TIME-BASE clock (40 MHz) or A/D sampling clock (TIMEBASE / SI_counter). When the count reaches 0, the counter stops and the card starts to acquire data. The total acquired data length = number of enable-channel * PSC_counter.
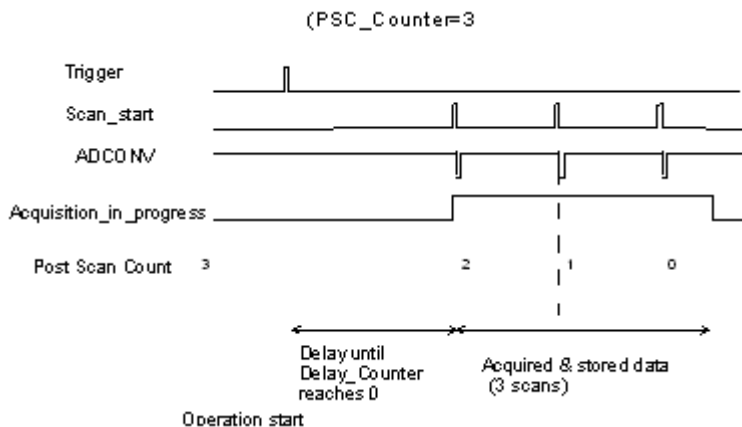

Figure 4-11: Delay trigger

NOTE	When the Delay_counter clock source is set to TIMEBASE, the maximum delay time = 216/40M s = 1.638ms, and the source is set to A/D sampling clock, the maximum delay time may be higher than 216 * SI_counter / 40M.

Post-Trigger or Delay-trigger Acquisition with re-trigger

Use post-trigger or delay-trigger acquisition with re-trigger function in applications where you want to collect data after several trigger events. The number of scans after each trigger is specified in PSC_counter, and users could program Retrig_no to specify the re-trigger numbers. Figure 4-12 illustrates an example. In this example, two scans of data is acquired after the first trigger signal, then the card waits for the re-trigger signal (re-trigger signals which occur before the first two scans is completed will be ignored). When the re-trigger signal occurs, two more scans are performed. The process repeats until specified amount of re-trigger signals are detected. The total acquired data length = number of enable-channel * PSC_counter * Re-trig_no.
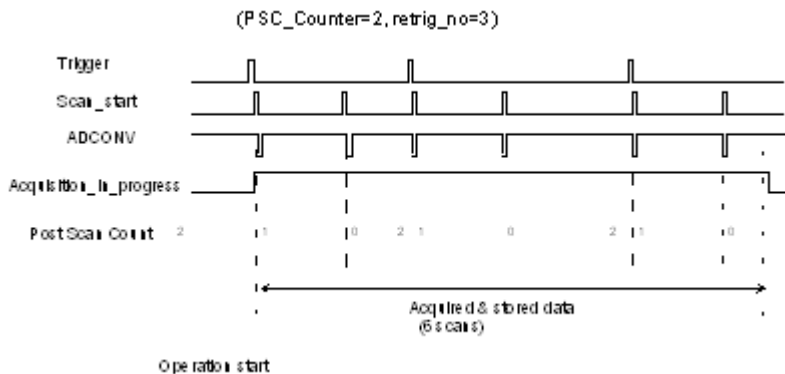

Figure 4-12: Post trigger with re-trigger

Bus-mastering DMA Data Transfer

PCI bus-mastering DMA is necessary for high speed DAQ in order to utilize the maximum PCI bandwidth. The bus-mastering controller, which is built in the PLX IOP-480 PCI controller, controls the PCI bus when it becomes the master of the bus. Bus mastering reduces the size of the on-board memory and reduces the CPU loading because data is directly transferred to the computer's memory without host CPU intervention.

Bus-mastering DMA provides the fastest data transfer rate on PCI-bus. Once the analog input operation starts, control returns to your program. The hardware temporarily stores the acquired data in the onboard AD Data FIFO and then transfers the data to a user-defined DMA buffer memory in the computer. Note that even when the acquired data length is less than the Data FIFO, the AD data is not kept in the Data FIFO but directly transferred into host memory by the bus-mastering DMA.

The DMA transfer mode is complicated to program. We recommend using a high-level program library to configure this card. If users would like to know more about software programs that can handle the DMA bus master data transfer, visit to http://www.plxtech.com for more information on PCI controllers.

By using a high-level programming library for high speed DMA data acquisition, you simply need to assign the sampling period and the number of conversion into your specified counters. After the AD trigger condition is matched, the data is transferred to the system memory by the bus-mastering DMA.

The PCI controller also supports the function of scatter/gather bus mastering DMA, which helps you transfer large amounts of data by linking all the memory blocks into a continuous linked list.

In a multi-user or multi-tasking OS, like Windows, Linux, etc, it is difficult to allocate a large continuous memory block to do the DMA transfer. Therefore, the PLX IOP-480 provides the function of scatter/gather or chaining mode DMA to link the non-continuous memory blocks into a linked list so that you can transfer very large amounts of data without being limited by the fragment of small size memory. You can configure the linked list for the input DMA channel or the output DMA channel.

Figure 4-13 shows a linked list that is constructed by three DMA descriptors. Each descriptor contains a PCI address, a local address, a transfer size, and the pointer to the next descriptor. You can allocate many small size memory blocks and chain their associative DMA descriptors altogether by their application programs. The PCI/PCIe/PXI-62010/62006/62005 card software driver provides simple settings for the scatter/gather function, including some sample programs in the JYTEK All-in-One CD.
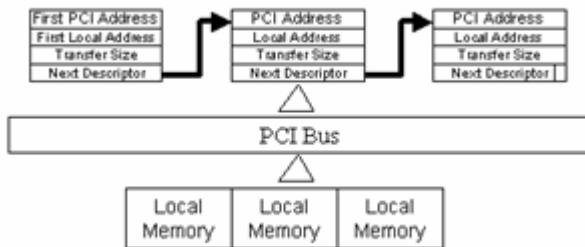

Figure 4-13: Scatter/gather DMA for data transfer

In non-chaining mode, the maximum DMA data transfer size is 2 M double words (8M bytes). However, by using chaining mode, scatter/gather, there is no limitation on the DMA data transfer size. You can also link the descriptor nodes circularly to achieve a multi-buffered mode DMA.

4.2   D/A Conversion

There are two 12-bit D/A output channels available in the PCI/PCIe/PXI-62010/62006/62005 card. When using D/A converters, you should assign and control the D/A converter reference sources for the D/A operation mode and D/A channels. You could also set the output polarity to unipolar or bipolar.

The reference selection control lets you utilize in full the multiplying characteristics of the D/A converters. Internal 10V reference and external reference inputs are available in the PCI/PCIe/PXI-62010/62006/62005 card. The range of the D/A output is directly related to the reference. The digital codes that are updated to the D/A converters will multiply with the reference to generate the analog output. While using internal 10V reference, the full range would be –10V to +9.9951V in the bipolar output mode, and 0V to 9.9976V in the unipolar output mode. While using an external reference, you can reach different output ranges by connecting different references. For example, if connecting a DC –5V with the external reference, then you can get a full range from –4.9976V to +5V in the bipolar output with inverting characteristics due to the negative reference voltage. You could also have an amplitude modulated (AM) output by feeding a sinusoidal signal into the reference input. The range of the external reference should be within ±10V. Table 4-5 and 4-6 illustrates the relationship between digital code and output voltages **with Vref=10V and if internal reference is selected**.

Digital Code	Analog Output
111111111111	Vref * (2047/2048)
100000000001	Vref * (1/2048)
100000000000	0V
011111111111	-Vref * (1/2048)
000000000000	-Vref

Table 4-5: Bipolar Output Code Table

Digital Code	Analog Output
111111111111	Vref * (4095/4096)

Table 4-6: Unipolar Output Code Table

Digital Code	Analog Output
100000000000	Vref * (2048/4096)
000000000001	Vref * (1/4096)
000000000000	0V

Table 4-6: Unipolar Output Code Table

The D/A conversion is initiated by a trigger source. You must decide how to trigger the D/A conversion. The data output will start when a trigger condition is met. Before the start of D/A conversion, D/A data is transferred from the computer's main memory to a buffering Data FIFO.

There are two modes of the D/A conversion: Software Update and Timed Waveform Generation. These are described below, including the timing, trigger source control, trigger modes, and data transfer methods. Either mode may be applied to D/A channels independently. You can software update DA CH0 while generating timed waveforms on CH1 at the same time.

Software Update

This is the easiest way to generate D/A output. To do this:

1. Specify the D/A output channels.

2. Set output polarity (unipolar or bipolar) and reference source (internal 10V or external AOEXTREF).

3. Update the digital values into D/A data registers through a software output command.

Timed Waveform Generation

This mode can provide your applications with a precise D/A output with a fixed update rate. It can be used to generate an infinite or finite waveform. You can accurately program the update period of the D/A converters.

The D/A output timing is provided through a combination of counters in the FPGA on board. There are a total of five counters to be specified. These counters include:

- ▶ UI_counter (24 bits): specify the DA Update Interval = CHUI_counter/TIMEBASE
- ▶ UC_counter (24 bits): specify the total Update Counts in a single waveform
- ▶ IC_counter (24 bits): specify the Iteration Counts of waveform
- ▶ DA_DLY1_counter (16 bits): specify the Delay from the trigger to the first update start
- ▶ DA_DLY2_counter (16 bits): specify the Delay between two consecutive waveform generations

Figure 4-14 shows a typical D/A timing diagram assuming the data in the data buffer are 2V, 4V, -4V, 0V. D/A updates its output on each rising edge of DAWR. The meaning of the counters enumerated above are discussed in the following sections.
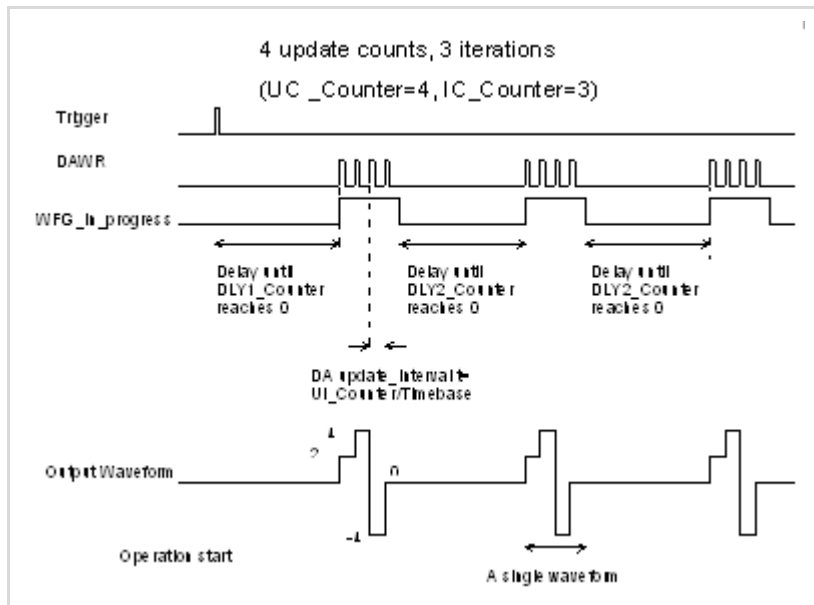
Figure 4-14: Typical D/A Timing of Waveform Generation

NOTE	The maximum D/A update rate is 1 MHz. Therefore, the minimum setting of the UI_counter is 40 while using an internal TIMEBASE (40 MHz).

Trigger Modes

Post-Trigger Generation

Use post-trigger when you want to perform DA waveform right after a trigger event occurs. In this trigger mode DLY1_Counter is ignored and not be specified. Figure 4-15 shows a single waveform generated right after a trigger signal is detected assuming the data in the data buffer are 2V, 4V, 6V, 3V, 0V, -4V, -2V, and 4V. The trigger signal could come from a software command, an analog trigger or a digital trigger. Refer to section 4.5 for detailed information.
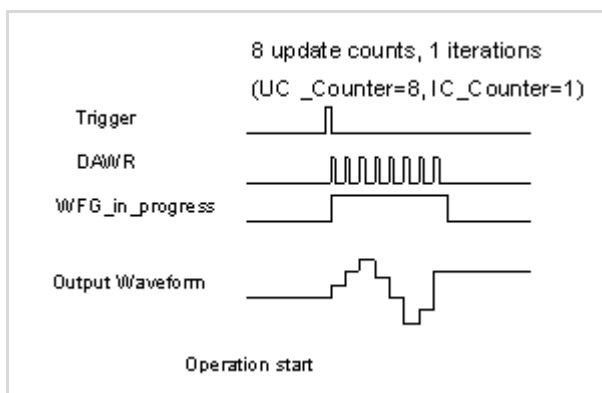

Figure 4-15: Post Trigger Waveform Generation

Delay-Trigger Generation

Use delay trigger when you want to delay the waveform generation after a trigger event. In Table 4-16, DA_DLY1_counter determines the delay time from the trigger signal to the start of the waveform generation, assuming the data in the data buffer are 2V, 4V, 6V, 3V, 0V, -4V, -2V, and 4V. DLY1_counter counts down on the rising edge of its clock source after the trigger condition is met. When the count reaches 0, the counter stops and the PCI/PCIe/PXI-62010/62006/62005 card starts the waveform generation. This DLY1_Counter is 16-bit wide and you can set the delay time in units of TIMEBASE (delay time = DLY1_Counter/TIME-

BASE) or in units of update period (delay time = DLY1_Counter * UI_counter/TIMEBASE), so the delay time can reach a wider range.
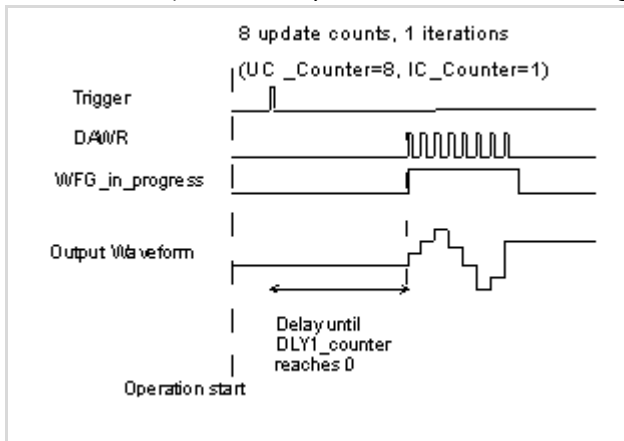

Figure 4-16: Delay Trigger Waveform Generation

Post-Trigger or Delay-Trigger with Re-trigger

Use post-trigger or delay-trigger with re-trigger function when you want to generate waveform after more than one trigger events. The re-trigger function can be enabled or disabled by software setting. In Figure 4-17, each trigger signal will initiate a waveform generation assuming the data in the data buffer are 2V, 4V, 2V, and 0V. However, the trigger event would be ignored while the waveform generation is ongoing.
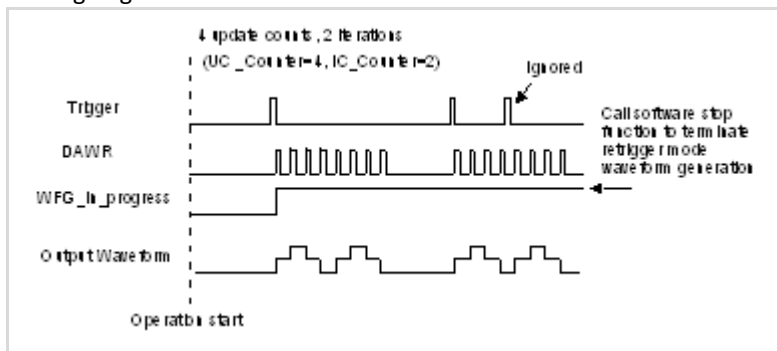

Figure 4-17: Re-triggered Waveform Generation

Iterative Waveform Generation

Set IC_Counter in order to generate iterative waveforms from the data of a single waveform. The counter stores the iteration number and the iterations may be finite (Figure 4-18) or infinite (Figure 4-19). Both figures assume that the data in the data buffer are 2V, 4V, 2V, and 0V.

A data FIFO on board is used to buffer the digital data for DA output. If the data size of a single waveform you specified (That is, Update Counts in UC_counter) is less than the FIFO size, after initially transferring the data from the host PC memory to the FIFO on board, the data in the FIFO will be automatically re-transmitted whenever a single waveform is completed. Therefore, it won't occupy the PCI bandwidth when repetitive waveforms are performed. However, if the size of a single waveform were larger than that of the FIFO, it needs to be intermittently loaded from the host PC's memory via DMA, when a repetitive waveforms is performed thus PCI bandwidth would be occupied.

The data FIFO size on PCI/PCIe/PXI-62010 is 2k samples and 512 samples on PCI/PCIe/PXI-62005/62006.
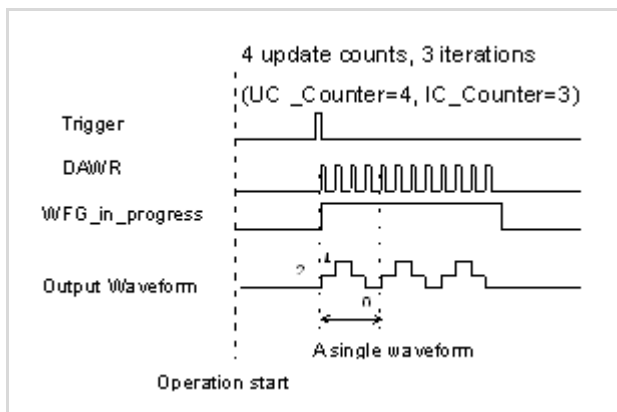

Figure 4-18: Finite Iterative Waveform Generation with Post-trigger and DLY2_Counter = 0
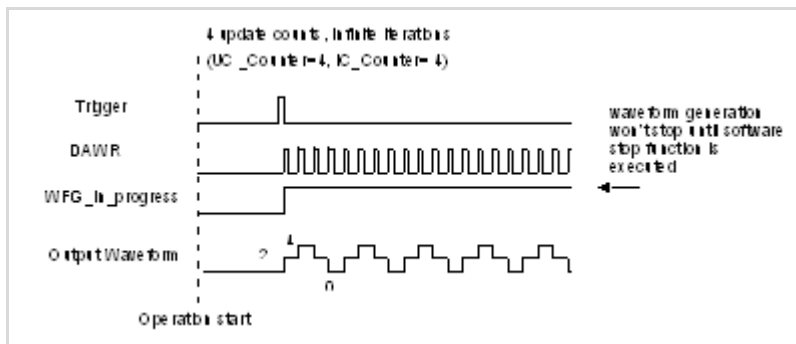
Figure 4-19: Infinite Iterative Waveform Generation with Post-trigger and DLY2_Counter = 0

NOTES   When running infinite iterative waveform generation, setting IC_Counter is ineffective to the waveform generation. It only makes a difference when setting Stop mode III. Refer to Figure 4-22.

Setting finite and infinite iterative waveform generation is not discussed in this manual. Refer to software documentation for related information.

Delay2 in Repetitive Waveform Generation

To diversify the D/A waveform generation, we add a DLY2 Counter to separate two consecutive waveforms in repetitive waveform generation. The time between two waveforms is set by the value of DLY2 Counter. The Delay2 counter starts to count down after a waveform generation finishes and the next waveform generation starts right after it counts down to zero, as shown in Figure 4-20. This DLY2_Counter is 16-bit wide and you may set the delay time in units of TIMEBASE (delay time = DLY2_Counter/TIMEBASE) or in units of update period (delay time = DLY2_Counter * UI_counter/TIMEBASE), so the delay time can reach a wider range.

Stop Modes of Scan Update

You can call software stop function to stop waveform generation when it is still in progress. Three stop modes are provided for timed waveform generation meant to stop the waveform generation. You can apply these three modes to stop waveform generation no matter infinite or finite waveform generation mode is selected.

Figure 4-20 illustrates an example for stop mode I, assuming the data in the data buffer are 2V, 4V, 2V, and 0V. In this mode, the waveform stops immediately when software command is asserted.

In stop mode II, after a software stop command is given, the waveform generation does not stop until a complete single waveform is finished. See Figure 4-21. Since the UC_counter is set to four, the total DA update counts (number of pulses of DAWR signal) must be a multiple of four (update counts = 20 in this example).

In stop mode III, after a software stop command is given, the waveform generation does not stop until the performed number of waveforms is a multiple of the IC_Counter. See Figure 4-22. Since the IC_Counter is set to three, the total generated waveforms must be a multiple of three (waveforms = 6 in this example), and the total DA update counts must be a multiple of 12 (UC_counter * IC_Counter). You can compare these three figures to see the differences.
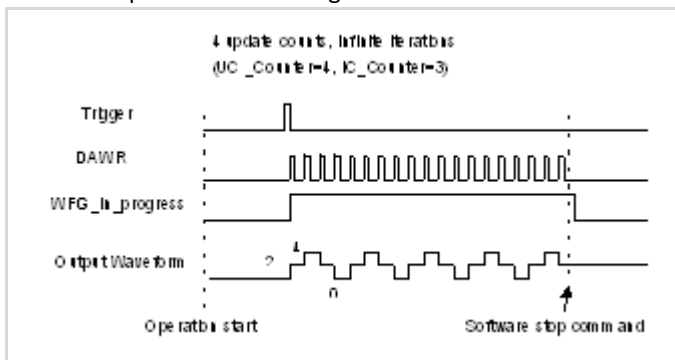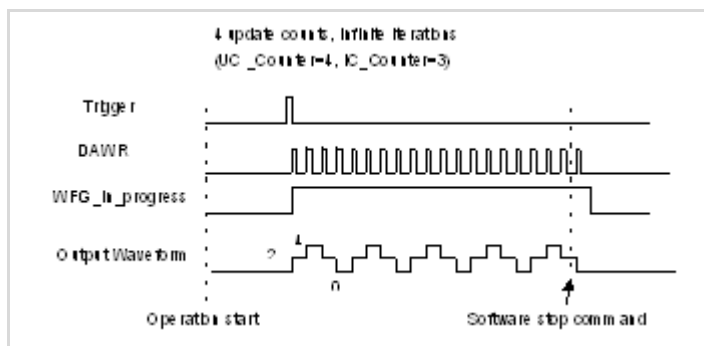

Figure 4-20: Stop Mode I
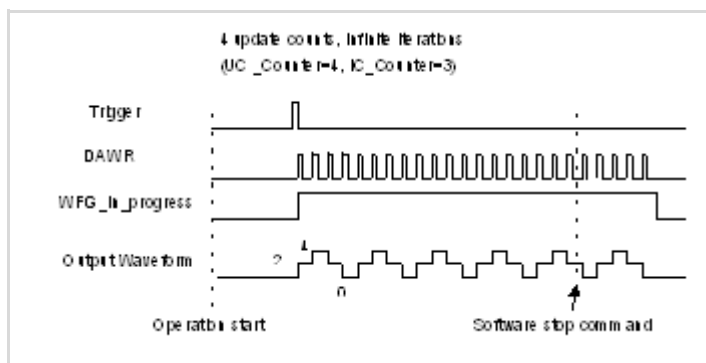
Figure 4-21: Stop Mode II

Figure 4-22: Stop Mode III

4.3 Digital I/O

The PCI/PCIe/PXI-62010/62006/62005 card contains 24 lines of general-purpose digital I/O (GPIO) which is provided through the 82C55A chip.

The 24-line GPIO are separated into three ports: Port A, Port B and Port C. Port A and Port B can be programmed to be either input or output ports. Port C can be separated into high bit (PC4-PC7) and low bit (PC0-PC3), and both high bit and low bit ports can be programmed for input or output. Upon system startup or reset, all the GPIO pins are reset to high impedance inputs.

The PCI/PCIe/PXI-62010 also provides two digital inputs per channel (SDI from J5), which are sampled simultaneously with an analog signal input and is stored with the 14-bit AD data. Refer to Figure 4.1 for the more details.

4.4 General Purpose Timer/Counter Operation

Two independent 16-bit up/down timer/counter are designed within FPGA for various applications. They have the following features:

- ▶ Count up/down controlled by hardware or software
- ▶ Programmable counter clock source (internal or external clock up to 10 MHz)
- ▶ Programmable gate selection (hardware or software control)
- ▶ Programmable input and output signal polarities (high active or low active)
- ▶ Initial count can be loaded from software
- ▶ Current count value can be read-back by software without affecting circuit operation

Timer/Counter functions basics

Each timer/counter has three inputs that can be controlled via hardware or software. They are clock input (GPTC_CLK), gate input (GPTC_GATE), and up/down control input (GPTC_UPDOWN). The GPTC_CLK input provides a clock source input to the timer/counter. Active edges on the GPTC_CLK input make the counter increment or decrement. The GPTC_UPDOWN input controls whether the counter counts up or down. The GPTC_GATE input is a control signal which acts as a counter enable or a counter trigger signal under different applications.

The output of timer/counter is GPTC_OUT. After power-up, GPTC_OUT is pulled high by a pulled-up resister about 10K ohms. Then GPTC_OUT goes low after the PCI/PCIe/PXI-62010/62006/62005 card is initialized.

All the polarities of input/output signals can be programmed by software. In this chapter, for easy explanation, all GPTC_CLK, GPTC_GATE, and GPTC_OUT are assumed to be active high or rising-edge triggered in the figures.

General Purpose Timer/Counter modes

Eight programmable timer/counter modes are provided. All modes start operating following a software-start signal that is set by the software. The GPTC software reset initializes the status of the counter and re-loads the initial value to the counter. The operation remains halted until the software-start is re-executed. The operating theories under different modes are described as below.

Mode 1: Simple Gated-Event Counting

In this mode, the counter counts the number of pulses on the GPTC_CLK after the software-start. Initial count can be loaded from software. Current count value can be read-back by software any time without affecting the counting. GPTC_GATE is used to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 4-23 illustrates the operation with initial count = 5, countdown mode.
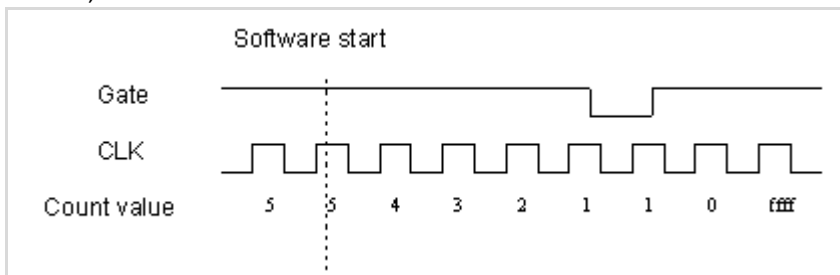

Figure 4-23: Mode 1 Operation

Mode 2: Single Period Measurement

In this mode, the counter counts the period of the signal on GPTC_GATE in terms of GPTC_CLK. Initial count can be loaded from software. After the software-start, the counter counts the number of

active edges on GPTC_CLK between two active edges of GPTC_GATE. After the completion of the period interval on GPTC_GATE, GPTC_OUT outputs high and then current count value can be read-back by software. Figure 4-24 illustrates the operation where initial count = 0, count-up mode.

Figure 4-24: Mode 2 Operation

Mode 3: Single Pulse-width Measurement

In this mode, the counter counts the pulse-width of the signal on GPTC_GATE in terms of GPTC_CLK. Initial count can be loaded from software. After the software-start, the counter counts the number of active edges on GPTC_CLK when GPTC_GATE is in its active state. After the completion of the pulse-width interval on GPTC_GATE, GPTC_OUT outputs high, then current count value can be read-back by software. Figure 4-25 illustrates the operation where initial count = 0, count-up mode.
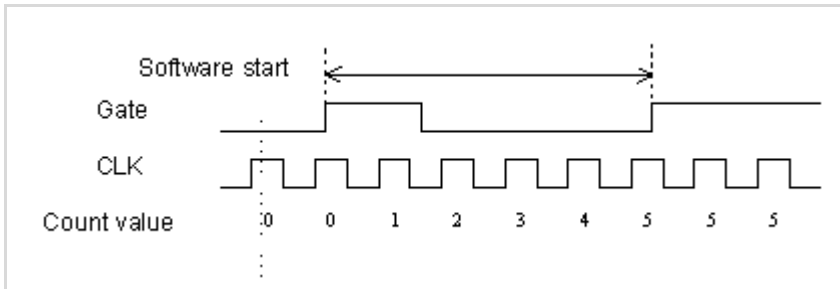

Figure 4-25: Mode 3 Operation

Mode 4: Single Gated Pulse Generation

This mode generates a single pulse with programmable delay and programmable pulse-width following the software-start. The two programmable parameters could be specified in terms of periods of the GPTC_CLK input by software. GPTC_GATE is used to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 4-26 illustrates the generation of a single pulse with a pulse delay of two and a pulse-width of four.
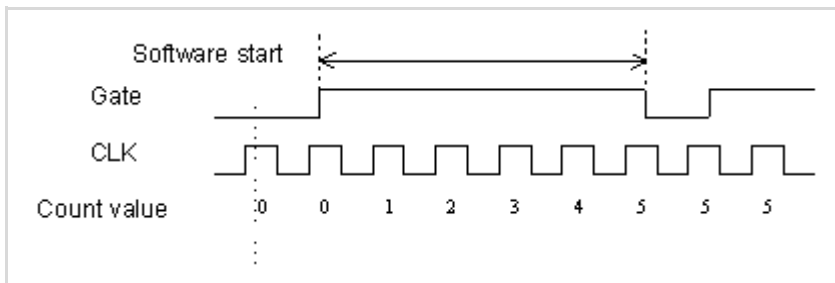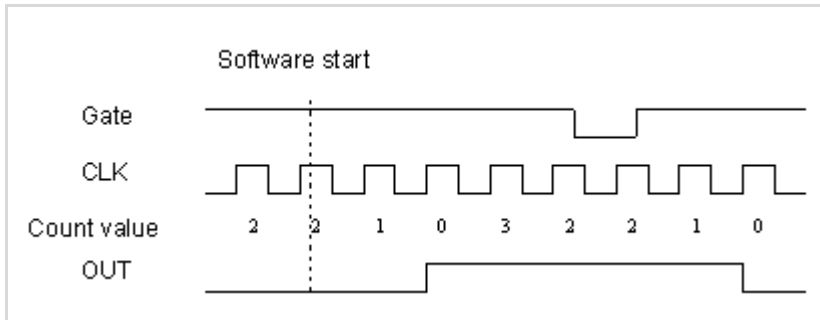

Figure 4-26: Mode 4 Operation

Mode 5: Single Triggered Pulse Generation

This function generates a single pulse with programmable delay and pro-grammable pulse-width following an active GPTC_GATE edge. You could specify these programmable parameters in terms of periods of the GPTC_CLK input. Once the first GPTC_GATE edge triggers the single pulse, GPTC_GATE takes no effect until the software-start is re-executed. Figure 4-27 illustrates the generation of a single pulse with a pulse delay of two and a pulse-width of four.

Figure 4-27: Mode 5 Operation

Mode 6: Re-triggered Single Pulse Generation

This mode is similar to Mode 5 except that the counter generates a pulse following every active edge of GPTC_GATE. After the software-start, every active GPTC_GATE edge triggers a single pulse with pro-grammable delay and pulse-width. Any GPTC_GATE triggers that occur when the prior pulse is not completed would be ignored. Figure 4-28 illustrates the generation of two pulses with a pulse delay of two and a pulse-width of four.
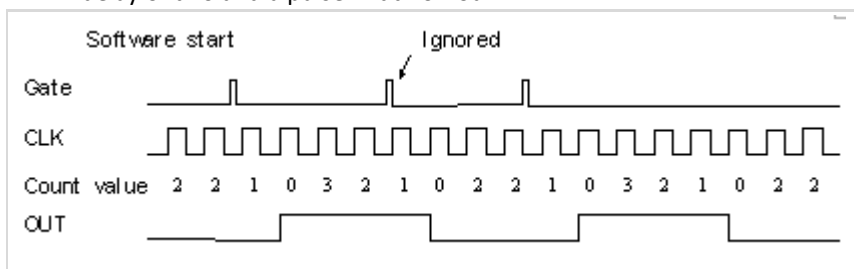
Figure 4-28: Mode 6 Operation

Mode 7: Single Triggered Continuous Pulse Generation

This mode is similar to Mode 5 except that the counter generates continuous periodic pulses with programmable pulse interval and pulse-width following the first active edge of GPTC_GATE. Once the first GPTC_GATE edge triggers the counter, GPTC_GATE takes no effect until the software-start is re-executed. Figure 4-29 illustrates the generation of two pulses with a pulse delay of four and a pulse-width of three.
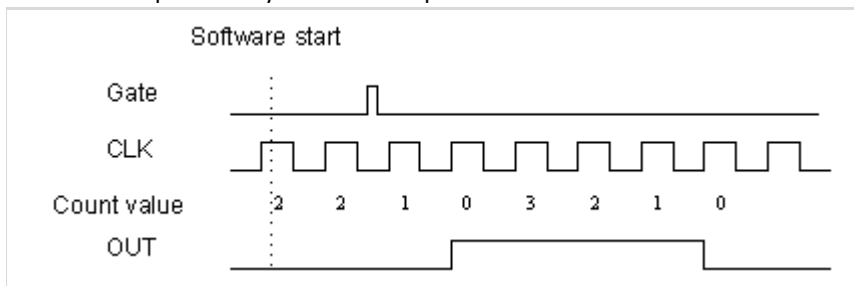

Figure 4-29: Mode 7 Operation

Mode 8: Continuous Gated Pulse Generation

This mode generates periodic pulses with programmable pulse interval and pulse-width following the software-start. GPTC_GATE is used to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 4-30 illustrates the generation of two pulses with a pulse delay of four and a pulse-width of three.

Figure 4-30: Mode 8 Operation
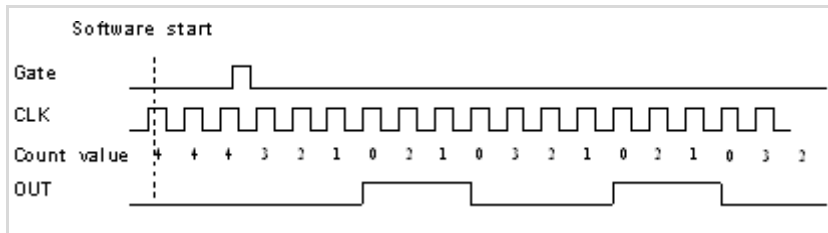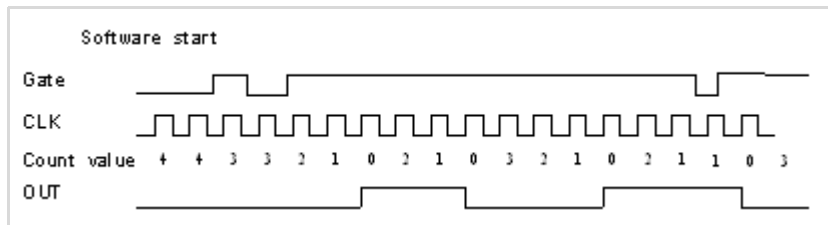
4.5 Trigger Sources

JYTEK provides flexible trigger selections in the PCI/PCIe/PXI-62010/ 62000 Series products. In addition to the internal software trigger, the PCI/PCIe/PXI-62010/62006/62005 card also supports external analog, digital triggers, and SSI triggers. You can configure the trigger source by software for A/D and D/A processes individually. Note that the A/D and the D/A conversion share the same analog trigger.

Software-Trigger

This trigger mode does not need any external trigger source. The trigger asserts right after you execute the specified function calls to begin the operation. A/D and D/A processes can receive an individual software trigger.

External Analog Trigger

The analog trigger circuitry routing is shown in the Figure 4-31. The analog multiplexer can select either a direct analog input from the EXTATRIG pin (SRC1 in Figure 4-31) in the 68-pin connector or the input signal of ADC (SRC2 in Figure 4-31). That is, one of the four channel inputs you can select as a trigger source. Both trigger sources can be used for all trigger modes. The range of trigger level for SRC1 is ±10V and the resolution is 78mV (refer to Table 4-6), while the trigger range of SRC2 is the full-scale range of the selected channel input and the resolution is the desired range divided by 256. For example, if the channel input selected to be the trigger source is set bipolar and ±5V range, the trigger voltage would be 4.96V when the trigger level code is set to 0xFF while 0V when the code is set to 0x80.
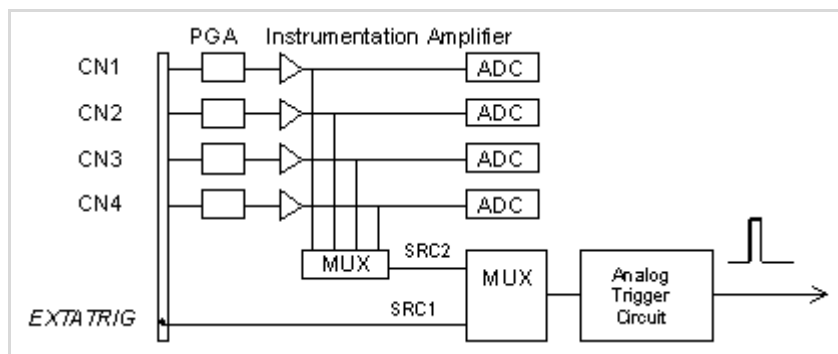
Figure 4-31: Analog Trigger Block Diagram

Trigger level digital setting	Trigger voltage
0xFF	9.92V
0xFE	9.84V
---	---
0x81	0.08V
0x80	0
0x7F	-0.08V
---	---
0x01	-9.92V

Table 4-7: Analog Trigger SRC1 (EXTATRIG) Ideal Transfer Characteristic

The trigger signal is generated when the analog trigger condition is satisfied. There are five analog trigger conditions in the PCI/PCIe/PXI-62010/62006/62005 card. The PCI/PCIe/PXI-62010/62006/62005 card uses two threshold voltages, Low_Threshold and High_Threshold to build the five different trigger conditions. You could configure the trigger conditions easily by software.

Below-Low Analog Trigger Condition

Figure 4-32 shows the below-low analog trigger condition, the trigger signal is generated when the input analog signal is less than the Low_Threshold voltage, and the High_Threshold setting is not used in this trigger condition.
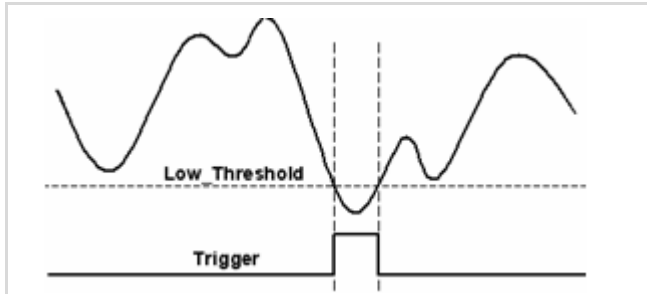
Figure 4-32: Below-Low Analog Trigger Condition

Above-High Analog Trigger Condition

Figure 4-33 shows the above-high analog trigger condition, the trigger signal is generated when the input analog signal is higher than the High_Threshold voltage, and the Low_Threshold setting is not used in this trigger condition.
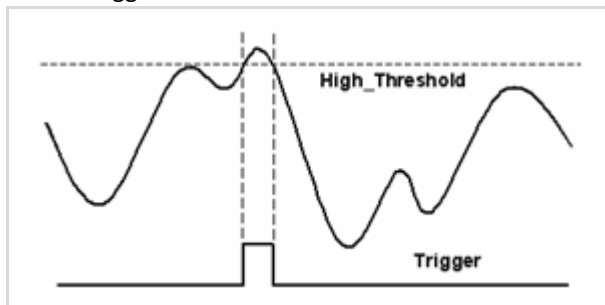
Figure 4-33: Above-High Analog Trigger Condition

Inside-Region analog trigger condition

Figure 4-34 shows the inside-region analog trigger condition, the trigger signal is generated when the input analog signal level falls in the range between the High_Threshold and the Low_Threshold voltages.

| NOTE | The High_Threshold setting should be always higher than the Low_Threshold voltage setting. |
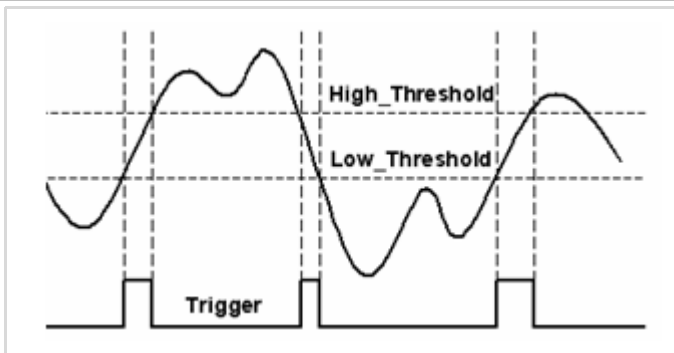
Figure 4-34: Inside-Region Analog Trigger Condition

High-Hysteresis analog trigger condition

Figure 4-35 shows the high-hysteresis analog trigger condition, the trigger signal is generated when the input analog signal level is greater than the High_Threshold voltage, and the Low_Threshold voltage determines the hysteresis duration. Note the High_Threshold setting should be always higher then the Low_Threshold voltage setting.

Figure 4-35: High-Hysteresis Analog Trigger Condition

Low-Hysteresis analog trigger condition

Figure 4-36 shows the low-hysteresis analog trigger condition, the trigger signal is generated when the input analog signal level is less than the Low_Threshold voltage, and the High_Threshold voltage determines the hysteresis duration. Note the High_Threshold setting should be always higher then the Low_Threshold voltage setting.

Figure 4-36: Low-Hysteresis Analog Trigger Condition

External Digital Trigger

An external digital trigger occurs when a rising edge or a falling edge is detected on the digital signal connected to the EXTDTRIG or the EXTWFTRG of the 68-pin connector for external digital trigger. The EXTDTRIG is dedicated for A/D process, and the EXTWFTRG is used for D/A process. You can program the trigger polarity using the software drivers. Note that the signal level of the external digital trigger signals should be TTL-compatible and the minimum pulse is 20 ns.

Figure 4-37: External Digital Trigger

4.6   User-controllable Timing Signals

In order to meet the requirements for user-specific timing and require-ments for synchronizing multiple cards, the PCI/PCIe/PXI-62010/62006/62005 card provides flexible user-controllable timing signals to connect to external circuitry or additional cards.

The whole DAQ timing of the PCI/PCIe/PXI-62010/62006/62005 card is composed of a bunch of counters and trigger signals in the FPGA. These timing signals are related to the A/D, D/A conversions, and Timer/Counter applications. These timing signals can be input to or output from the I/O connectors, SSI connector, and the PXI bus. Therefore, the internal timing signals can be used to control external devices or cir-cuitry. Note that in other models of PCI/PCIe/PXI-62010/62006/62005 card, the user-controllable timing signals may vary. However, the SSI/PXI timing signals remain the same for every PCI/PCIe/PXI-62010/62006/62005 card.

We implemented signal multiplexers in the FPGA to individually choose the desired timing signals for the DAQ operations, as shown in the Figure 4-38

Figure 4-38: DAQ signals routing

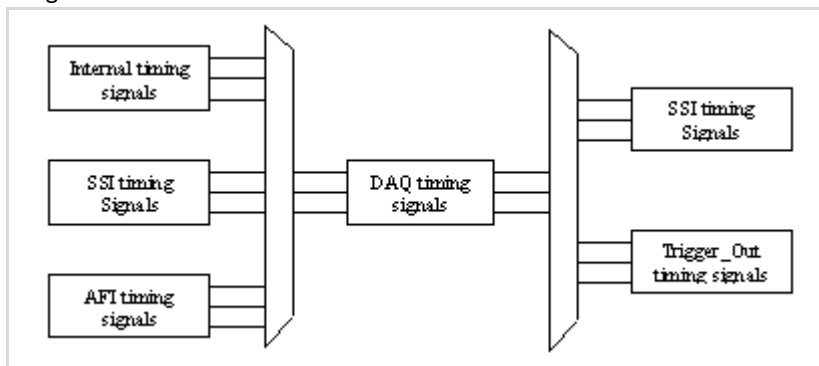You can utilize the flexible timing signals through our software drivers, then simply and correctly connect the signals with the PCI/PCIe/PXI-62010/62006/62005 cards. Here is the summary of the DAQ timing sig-nals and the corresponding functionalities for PCI/PCIe/PXI-62010/62006/62005 card.

Timing signal category	Corresponding functionality
SSI/PXI signals	Multiple cards synchronization
AFI signals	Control PCI-62000 by external timing signals
AI_Trig_Out, AO_Trig_Out	Control external circuitry or boards

Table 4-8: User-controllable Timing Signals and Functionalities

DAQ timing signals

The user-controllable internal timing-signals contain (refer to section 4.1 for the internal timing signal definition):

1. TIMEBASE, providing TIMEBASE for all DAQ operations, which could be from internal 40 MHz oscillator, EXTTIMEBASE from I/O connector or the SSI_TIMEBASE. Note that the frequency range of the EXTTIMEBASE is 1 MHz to 40 MHz, and the EXT-TIMEBASE should be TTL-compatible.

2. AD_TRIG, the trigger signal for the A/D operation, which could come from external digital trigger, analog trigger, internal software trigger, and SSI_AD_TRIG. Refer to section 4.5 for detailed description.

3. SCAN_START, the signal to start a scan, which would bring the following ADCONV signals for AD conversion, and could come from the internal SI_counter, AFI[0] and SSI_AD_START. This signal is synchronous to the TIMEBASE. Note that the AFI[0] should be TTL-compatible and the minimum pulse width should be the pulse width of the TIMEBASE to guarantee correct functionalities.

4. ADCONV, the conversion signal to initiate a single conversion, which could be derived from internal counter, AFI[0] or SSI_ADCONV. Note that this signal is edge-sensitive. When using AFI[0] as the external ADCONV source, each rising edge of AFI[0] would bring an effective conversion signal. Also note that the AFI[0] signal should be TTL-compatible and the minimum pulse width is 20 ns.

5. DA_TRIG, the trigger signal for the D/A operation, which could be derived from external digital trigger, analog trigger,

internal software trigger, and SSI_AD_TRIG. Refer to section 4.5 for detailed description.

6. DAWR, the update signal to initiate a single D/A conversion, which could be derived from internal counter, AFI[1] or SSI_DAWR. Note that this signal is edge-sensitive. When using AFI[1] as the external DAWR source, each rising edge of AFI[1] would bring an effective update signal. Also note that the AFI[1] signal should be TTL-compatible and the minimum pulse width is 20 ns.

Auxiliary Function Inputs (AFI)

You can use the AFI in applications that take advantage of external circuitry to directly control the PCI/PCIe/PXI-62010/62006/62005 card. The AFI includes two categories of timing signals: one group is the dedicated input, and the other is the multi-function input. Table 4-9 illustrates this categorization.

Category	Timing signal	Functionality	Constraints
Dedicated input	EXTTIMEBASE	Replace the internal TIMEBASE	1. TTL-compatible
			2. 1MHz to 40MHz
			3. Affects on both A/D and D/A operations
	EXTDTRIG	External digital trigger input for A/D operation	1. TTL-compatible
			2. Minimum pulse width = 20ns
			3. Rising edge or falling edge
	EXTWFTRG	External digital trigger input for D/A operation	1. TTL-compatible
			2. Minimum pulse width = 20ns
			3. Rising edge or falling edge

Table 4-9: Auxiliary Function Input Signals and Functionalities

Category	Timing signal	Functionality	Constraints
Multi-function input	AFI[0] (Dual functions)	Replace the internal ADCONV	1. TTL-compatible
			2. Minimum pulse width = 20ns
			3. Rising–edge sensitive only
		Replace the internal SCAN_START	1. TTL-compatible
			2. Minimum Pulse width > 2/TIMEBASE
	AFI[1]	Replace the internal DAWR	1. TTL-compatible
			2. Minimum pulse width = 20ns
			3.Rising–edge sensitive only

Table 4-9: Auxiliary Function Input Signals and Functionalities

EXTDTRIG and EXTWFTRIG

EXTDTRIG and EXTWFTRIG are dedicated digital trigger input signals for A/D and D/A operations respectively. Refer to section 4.5 for details.

EXTTIMEBASE

When the applications needs specific sampling frequency or update rate that the card could not generate from its internal TIMEBASE — the 40 MHz clock — you could utilize the EXTTIMEBASE with internal counters to achieve the specific timing intervals for both A/D and D/A operations. Note that once you choose the TIMEBASE source, both A/D and D/A operations will be affected because A/D and D/A operations share the same TIMEBASE.

AFI[0]

Alternatively, you can also directly apply an external A/D conversion signal to replace the internal ADCONV signal. This is another way to achieve customized sampling frequencies. The external ADCONV signal can only be inputted from the AFI[0]. As section 4.1 describes, the SI_counter triggers the generation of the A/D conversion signal, ADCONV, but when using the AFI[0] to replace the internal ADCONV signal, the SI_counter and the internally generated SCAN_START is not effective. By controlling the ADCONV externally, you can sample the data according to external events. In this mode, the Trigger signal and trigger mode settings are not available.

AFI[0] could also be used as SCAN_START signal for A/D operations. Refer to section 4.1 and section 4.6 for detailed descriptions of the SCAN_START signal. When using external signal (AFI[0]) to replace the internal SCAN_START signal, the pulse width of the AFI[0] must be greater than two time of the period of Timebase. This feature is suitable for the PCI-62200/PCIe-62200/PXI-62200 Series, which can scan multiple channels data controlled by an external event. Note that the AFI[0] is a multi-purpose input, and it can only be utilized for one function at any one time.

AFI[1]

Regarding the D/A operations, users could directly input the external D/A update signal to replace the internal DAWR signal. This is another way to achieve customized D/A update rates. The external DAWR signal can only be inputted from the AFI[1]. Note that the AFI[1] is a multi-purpose input, and it can only be utilized for one function at any one time. AFI[1] currently only has one function. JYTEK reserves it for future development.

System Synchronization Interface

SSI (System Synchronization Interface) provides the DAQ timing synchronization between multiple cards. In PCI/PCIe/PXI-62010/62006/62005 card, we designed a bi-directional SSI I/O to provide flexible connection between cards and allow one SSI master to output the signal and up to three slaves to receive the SSI signal. Note that the SSI signals are designed for card synchronization only and not for external devices.

SSI timing signal	Functionality
SSI_TIMEBASE	SSI master: send the TIMEBASE out
	SSI slave: accept the SSI_TIMEBASE to replace the internal TIMEBASE signal.
	Note: Affected on both A/D and D/A operations
SSI_AD_TRIG	SSI master: send the internal AD_TRIG out
	SSI slave: accept the SSI_AD_TRIG as the digital trigger signal.

Table 4-10: SSI Timing Signals Functionalities

SSI timing signal	Functionality
SSI_ADCONV	SSI master: send the ADCONV out
	SSI slave: accept the SSI_ADCONV to replace the internal ADCONV signal.
SSI_SCAN_START	SSI master: send the SCAN_START out
	SSI slave: accept the SSI_SCAN_START to replace the internal SCAN_START signal.
SSI_DA_TRIG	SSI master: send the DA_TRIG out.
	SSI slave: accept the SSI_DA_TRIG as the digital trigger signal.
SSI_DAWR	SSI master: send the DAWR out.
	SSI slave: accept the SSI_DAWR to replace the internal DAWR signal.

Table 4-10: SSI Timing Signals Functionalities

In PCI form factor, there is a connector on the top right corner of the card for the SSI. Refer to section 2.3 for the connector position. All the SSI signals are routed to the 20-pin connector from the FPGA. To synchronize multiple cards, users can connect a special ribbon cable (ACL-SSI) to all the cards in a daisy-chain configuration.

In PXI form factor, we utilize the PXI trigger bus built on the PXI backplane to provide the necessary timing signal connections. All the SSI signals are routed to the P2 connector. No additional cable is needed. For detailed information of the PXI specifications, refer to the PXI Specification Revision 2.0 from PXI System Alliance (www.pxisa.org).

The six internal timing signals could be routed to the SSI or the PXI trigger bus through software drivers. Refer to section 4.6 for detailed information on the six internal timing signals. Physically the signal routings are accomplished in the FPGA. Cards that are connected together through the SSI or the PXI trigger bus, will still achieve synchronization on the six timing signals.

The mechanism of the SSI/PXI

▶ We adopt master-slave configuration for SSI/PXI. In a system, for each timing signal, there shall be only one master, and other cards are SSI slaves or with the SSI function disabled.

▶ For each timing signal, the SSI master does not have to be in a single card.

For example:

We want to synchronize the A/D operation through the ADCONV signal for four PCI/PCIe/PXI-62010/62006/62005 cards. Card 1 is the master, and Card 2, 3, 4 are slaves. Card 1 receives an external digital trigger to start the post trigger mode acquisition. The SSI setting could be:

- ▶ Set the SSI_ADCONV signal of Card 1 to be the master.
- ▶ Set the SSI_ADCONV signals of Card 2, 3, 4 to be the slaves.
- ▶ Set external digital trigger for Card 1's A/D operation.
- ▶ Set the SI_counter and the post scan counter (PSC) of all other cards.
- ▶ Start DMA operations for all cards, so all the cards are waiting for the trigger event.

When the digital trigger condition of Card 1 occurs, Card 1 will internally generate the ADCONV signal and output this ADCONV signal to SSI_AD-CONV signal of Card 2, 3 and 4 through the SSI/PXI connectors. Thus we can achieve 16-channel acquisition simultaneously.

You could arbitrarily choose each of the six timing signals as the SSI master from any one of the cards. The SSI master can output the internal timing signals to the SSI slaves. With the SSI, users could achieve better card-to-card synchronization.

Note that when power-up or reset, the DAQ timing signals are reset to use the internal generated timing signals.

AI_Trig_Out and AO_Trig_Out

AI_Trig_Out (or AO_Trig_Out) is the signal output following one of the four trigger sources: software trigger, analog trigger, digital trigger, and SSI trigger selected by the user. That is, AI_Trig_Out follows the A/D trigger source, and AO_Trig_Out follows the D/A trigger source. These two signals can be used to control external peripheral circuits or boards, or can be used as synchronization control signals. The signal level of the AI_Trig_Out and AO_Trig_Out are TTL-compatible.

NOTE	AI_Trig_Out and AO_Trig_Out are output pins on J5 (68-pin VHDCI). Connecting them to any signal source may cause permanent damage to the card.

5 Calibration

This chapter introduces the calibration process to minimize AD measurement errors and DA output errors.

5.1 Loading Calibration Constants

The PCI/PCIe/PXI-62010/62006/62005 card is factory-calibrated before shipment. The associated calibration constants of the TrimDACs firmware to the onboard EEPROM. TrimDACs are devices containing multiple DACs within a single package. TrimDACs do not have memory capability. That means the calibration constants do not retain their values after the system power is turned off. Loading calibration constants is the process of loading the values of TrimDACs firmware stored in the onboard EEPROM. JYTEK provides a software utility that automatically reads the calibration constants automatically, if necessary.

There is a dedicated space for storing calibration constants in the EEPROM. In addition to the default bank of factory calibration constants, there is one user-utilization bank. This bank allows you to load the Trim-DACs firmware values either from the original factory calibration or from a subsequently-performed calibration.

Because of the fact that measurements and outputs errors may vary depending on time and temperature, it is recommended that you calibrate the card when it is integrated in your computing environment. The auto-calibration function is presented in the following sections.

5.2 Auto-calibration

Through the PCI/PCIe/PXI-62010/62006/62005 card auto-calibration feature, the calibration software measures and corrects almost all calibration errors without any external signal connections, reference voltage, or measurement devices.

The PCI/PCIe/PXI-62010/62006/62005 card comes with an onboard calibration reference to ensure the accuracy of auto-calibration. The reference voltage is measured in the production line through a digital potentiometer and compensated in the software. The calibration constant is memorized after this measurement. We do not recommended adjustment of the onboard calibration reference except when an ultra-precision calibrator is available.

NOTES
- Warm the card up for at least 15 minutes before initiating auto-calibration.
- Remove the cable before auto-calibrating the card since the DA outputs are changed during the process.

5.3 Saving Calibration Constants

When auto-calibration is completed, you can save the new calibration constants to the user-configurable banks in the EEPROM. The date and the temperature when you ran auto-calibration is saved with the calibration constants. You can store three sets of calibration constants according to three different environments and re-load the calibration constants later.

Warranty Policy

Thank you for choosing JYTEK. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. All JYTEK products come with a limited two-year warranty:

   ▶ The warranty period starts on the day the product is shipped from JYTEK's factory.

   ▶ Peripherals and third-party products not manufactured by JYTEK will be covered by the original manufacturers' warranty.

   ▶ For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. JYTEK is not responsible for any loss of data.

   ▶ Please ensure the use of properly licensed software with our systems. JYTEK does not condone the use of pirated software and will not service systems using such software. JYTEK will not be held legally responsible for products shipped with unlicensed software installed by the user.

   ▶ For general repairs, please do not include peripheral accessories. If peripherals need to be included, be certain to specify which items you sent on the RMA Request & Confirmation Form. JYTEK is not responsible for items not listed on the RMA Request & Confirmation Form.

2. Our repair service is not covered by JYTEK's guarantee in the following situations:

   ▶ Damage caused by not following instructions in the User's Manual.

   ▶ Damage caused by carelessness on the user's part during product transportation.

   ▶ Damage caused by fire, earthquakes, floods, lightening, pollution, other acts of God, and/or incorrect usage of voltage transformers.

   ▶ Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).

   ▶ Damage caused by leakage of battery fluid during or after change of batteries by customer/user.

   ▶ Damage from improper repair by unauthorized JYTEK technicians.

   ▶ Products with altered and/or damaged serial numbers are not entitled to our service.

   ▶ This warranty is not transferable or extendible.

   ▶ Other categories not protected under our warranty.

3. Customers are responsible for shipping costs to transport damaged products to our company or sales office.

If you have any further questions, please email our service center: service@jytek.com.

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