



JYTEK



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# PCI/PCIe/PXI- 62204/62205/62206/62208

64-/96-CH High Performance  
Multi-Function Data Acquisition Card  
**User's Manual**



**Manual Rev.** 1.0.1

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Advance Technologies; Automate the World.

# Using this manual

## 1.1 Copyright

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## 1.2 Audience and scope

This manual guides you when using JYTEK multi-function PCI/PCIe/PXI-62204/62205/62206/62208 card. The card's hardware, signal connections, and calibration information are provided for faster application building. This manual is intended for computer programmers and hardware engineers with advanced knowledge of data acquisition and high-level programming.

## 1.3 How this manual is organized

This manual is organized as follows:

**Chapter 1 Introduction:** This chapter introduces the PCI/PCIe/PXI-62204/62205/62206/62208 card including its features, specifications and software support information.

**Chapter 2 Installation:** This chapter presents the card's layout, package contents, and installation.

**Chapter 3 Signal Connections:** This part describes the PCI/PCIe/PXI-62204/62205/62206/62208 card signal connections.

**Chapter 4 Operation Theory:** The operation theory of the PCI/PCIe/PXI-62204/62205/62206/62208 card functions including A/D conversion, D/A conversion, and programmable function I/O are discussed in this chapter.

**Chapter 5 Calibration:** The chapter offers information on how to calibrate the PCI/PCIe/PXI-62204/62205/62206/62208 card for accurate data acquisition and output.

**Warranty Policy:** This presents the JYTEK Warranty Policy terms and coverages.

**Getting Service:** Contact information for JYTEK's worldwide offices.

## 1.4 Conventions

Take note of the following conventions used throughout the manual to make sure that you perform certain tasks and instructions properly.

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**NOTE** Additional information, aids, and tips that help you perform particular tasks.

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**IMPORTANT** Critical information and instructions that you **MUST** perform to complete a task.

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**WARNING** Information that prevents physical injury, data loss, module damage, program corruption etc. when trying to complete a particular task.

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# 1 Introduction

The PCI/PCIe/PXI-62204/62205/62206/62208 card is an advanced data acquisition card based on the 32-bit PCI or PCI Express<sup>®</sup> architecture. High performance designs and state-of-the-art technology make these cards ideal for data logging and signal analysis applications in medical, process control, etc.

## 1.1 Features

The PCI/PCIe/PXI-62204/62205/62206/62208 advanced data acquisition card has the following features:

- ▶ 32-bit PCI bus (PCI/PXI models) or PCI Express (PCIe model), plug and play
- ▶ Up to 96 single-ended inputs or 48 differential inputs supporting combinations of SE and DI analog input signals
- ▶ Up to 1024 words analog input Channel Gain Queue configuration size
- ▶ Analog input resolution and sampling rate:
  - ▷ PCI/PCIe/PXI-62204/62208: 12-bit and up to 3 MHz
  - ▷ PCI/PCIe/PXI-62205: 16-bit and up to 500 KHz
  - ▷ PCI/PCIe/PXI-62206: 16-bit and up to 250 KHz
- ▶ Programmable bipolar/unipolar analog input
- ▶ Programmable gain:
  - ▷ PCI/PCIe/PXI-62204/62208: x1, x2, x4, x5, x8, x10, x20, x40, x50, x200
  - ▷ PCI/PCIe/PXI-62205/62206: x1, x2, x4, x8
- ▶ A/D FIFO size: 1024 samples
- ▶ Versatile trigger sources: software trigger, external digital trigger, analog trigger and trigger from System Synchronization Interface (SSI)
- ▶ A/D data transfer: software polling and bus-mastering DMA with scatter/gather functionality
- ▶ Four A/D trigger modes including post-trigger, delay-trigger, pre-trigger and middle-trigger
- ▶ Two-channel D/A outputs with waveform generation capability (except PCI/PCIe/PXI-62208)
- ▶ 1024 word length output data FIFO for D/A channels
- ▶ D/A data transfer: Software update and bus-mastering DMA with scatter/gather functionality
- ▶ Support System Synchronization Interface (SSI)
- ▶ Full A/D and D/A auto-calibration
- ▶ Jumper-free and software-configurable

## 1.2 Applications

- ▶ Automotive Testing
- ▶ Cable Testing
- ▶ Transient signal measurement
- ▶ ATE
- ▶ Laboratory Automation
- ▶ Biotech measurement

## 1.3 Specifications

### Analog Input (AI)

- ▶ Programmable channels:
  - ▷ PCI/PCIe/PXI-62204/62205/62206: 64 single-ended (SE) or 32 differential input (DI)
  - ▷ PCI/PCIe/PXI-62208: 96 single-ended (SE) or 48 differential input (DI)
  - ▷ Mixing of SE and DI analog signal sources (Software selectable per channel)
- ▶ A/D converter:
  - ▷ PCI/PCIe/PXI-62204/62208: LT1412 or equivalent
  - ▷ PCI/PCIe/PXI-62205: A/D7665 or equivalent
  - ▷ PCI/PCIe/PXI-62206: A/D7663 or equivalent
- ▶ Max sampling rate:
  - ▷ PCI/PCIe/PXI-62204/62208: 3 MS/s (single-channel)  
1 MS/s (multi-channel)
  - ▷ PCI/PCIe/PXI-62205: 500 kS/s
  - ▷ PCI/PCIe/PXI-62206: 250 kS/s
- ▶ Resolution:
  - ▷ PCI/PCIe/PXI-62204/62208: 12-bit, no missing code
  - ▷ PCI/PCIe/PXI-62205/62206: 16-bit, no missing code
- ▶ Input coupling: DC
- ▶ FIFO buffer size:
  - ▷ PCI/PCIe/PXI-62204: 8K samples
  - ▷ PCI/PCIe/PXI-62205/62206/62208: 512 samples

- ▶ Programmable input range:

Device	Bipolar input range	Unipolar input range
62204/ 62208	$\pm 10$ V	—
	$\pm 5$ V	0 to 10 V
	$\pm 2.5$ V	0 to 5 V
	$\pm 2$ V	0 to 4 V
	$\pm 1.25$ V	0 to 2.5 V
	$\pm 1$ V	0 to 2 V
	$\pm 0.5$ V	0 to 1 V
	$\pm 0.25$ V	0 to 0.5 V
	$\pm 0.2$ V	0 to 0.4 V
	$\pm 0.05$ V	0 to 0.1 V
62205/ 62206	$\pm 10$ V	0 to 10 V
	$\pm 5$ V	0 to 5 V
	$\pm 2.5$ V	0 to 2.5 V
	$\pm 1.25$ V	0 to 1.25 V

**Table 1-1: Programmable Input Range**

- ▶ Operational common mode voltage range:  $\pm 11$ V
- ▶ Over-voltage protection:
  - ▷ Power on: Continuous  $\pm 30$ V
  - ▷ Power off: Continuous  $\pm 15$ V
- ▶ FIFO buffer size: 1024 samples
- ▶ Data transfers:
  - ▷ Programmed I/O
  - ▷ Bus-mastering DMA with scatter/gather
- ▶ Channel Gain Queue configuration size:
  - ▷ PCI/PCIe/PXI-62204/62205/62206: 512 words
  - ▷ PCI/PCIe/PXI-62208: 1024 words

► Bandwidth (Typical 25°C):

Device	Input range		Small signal bandwidth (-3dB)	Large signal bandwidth (1% THD)
62204/ 62208	±10 V	—	2000 kHz	—
	±5 V	0 V to 10 V		
	±2.5 V	0 V to 5 V		
	±1.25 V	0 V to 2.5 V		
	±2 V	0 V to 4 V	1450 kHz	—
	±0.5 V	0 V to 1 V		
	±1 V	0 V to 2 V	990 kHz	—
	±0.25 V	0 V to 0.5 V		
	±0.2 V	0 V to 0.4 V	240 kHz	—
	±0.05 V	0 V to 0.1 V		
62205	±10 V	0 V to 0 V	1600 kHz	300 kHz
	±5 V	0 V to 5 V	1400 kHz	310 kHz
	±2.5 V	0 V to 2.5 V	1000 kHz	310 kHz
	±1.25 V	0 V to 1.25 V	600 kHz	330 kHz
62206	±10 V	0 V to 10 V	760 kHz	300 kHz
	±5 V	0 V to 5 V	720 kHz	310 kHz
	±2.5 V	0 V to 2.5 V	610 kHz	310 kHz
	±1.25 V	0 V to 1.25 V	450 kHz	330 kHz

**Table 1-2: Bandwidth**

► System Noise (LSBrms, including Quantization, Typical, 25°C)

Device	Input Range	System Noise	Input Range	System Noise
62205	±10 V	0.95 LSBrms	0 V to 10 V	1.5 LSBrms
	±5 V	1.0 LSBrms	0 V to 5 V	1.6 LSBrms
	±2.5 V	1.1 LSBrms	0 V to 2.5 V	1.7 LSBrms
	±1.25 V	1.3 LSBrms	0 V to 1.25 V	1.9 LSBrms
62206	±10 V	0.8 LSBrms	0 V to 10 V	0.9 LSBrms
	±5 V	0.85 LSBrms	0 V to 5 V	1.0 LSBrms
	±2.5 V	0.85 LSBrms	0 V to 2.5 V	1.0 LSBrms
	±1.25 V	0.9 LSBrms	0 V to 1.25 V	1.2 LSBrms

**Table 1-3: System Noise**

► Input impedance:

- ▷ Normal power on: 1 G $\Omega$ /100 pF
- ▷ Power off: 820  $\Omega$
- ▷ Overload: 820  $\Omega$

► CMRR (DC to 60 Hz, Typical)

Device	Input Range	CMRR	Input Range	CMRR
62204/ 62208	All ranges	90 dB	—	—
62205/ 62206	±10 V	83 dB	0 V to 10 V	87 dB
	±5 V	87 dB	0 V to 5 V	90 dB
	±2.5 V	90 dB	0 V to 2.5 V	92 dB
	±1.25 V	92 dB	0 V to 1.25 V	93 dB

**Table 1-4: CMRR (DC to 60 Hz)**

► Settling time to full-scale step (Typical, 25°C):

Device	Input Range	Condition	Settling time		
62204/ 62208	±10 V		<ul style="list-style-type: none"> <li>Multiple channels, multiple ranges.</li> <li>All samples in unipolar/bipolar mode.</li> </ul>	1 μs to 0.1% error	
	±5 V	0 to 10 V			
	±2.5 V	0 to 5 V			
	±2 V	0 to 4 V			
	±1.25 V	0 to 2.5 V			
	±0.5 V	0 to 1 V			
	62204/ 62208	±10 V		<ul style="list-style-type: none"> <li>Multiple channels, multiple ranges.</li> <li>All samples in unipolar/bipolar mode.</li> </ul>	1.25 μs to 0.1% error
		±5 V	0 to 10 V		
		±2.5 V	0 to 5 V		
		√2 V	0 to 4 V		
		±1.25 V	0 to 2.5 V		
		±0.5 V	0 to 1 V		
	62204/ 62208	±1 V	0 to 2 V	<ul style="list-style-type: none"> <li>Multiple channels, multiple ranges.</li> <li>All samples in unipolar/bipolar mode.</li> </ul>	2 μs to 0.1% error
		±0.25 V	0 to 0.5 V		
±0.2 V		0 to 0.4 V	<ul style="list-style-type: none"> <li>Multiple channels, multiple ranges.</li> <li>All samples in unipolar/bipolar mode.</li> </ul>	5 μs to 0.1% error	
±0.05 V		0 to 0.1 V			
62205/ 62206	All Ranges		<ul style="list-style-type: none"> <li>Multiple channels, multiple ranges.</li> <li>All samples in unipolar/bipolar mode.</li> </ul>	2 μs to 0.1% error, 4 μs to 0.01% error	
	All Ranges				<ul style="list-style-type: none"> <li>Multiple channels, multiple ranges.</li> <li>All samples in unipolar/bipolar mode.</li> </ul>

**Table 1-5: Settling Time to Full Scale Step**

- ▶ Time-base source:
  - ▷ Internal 40 MHz or external clock Input ( $f_{\max}$ : 40 MHz,  $f_{\min}$ : 1 MHz, 50% duty cycle)
- ▶ Trigger modes: Post-trigger, delay-trigger, pre-trigger and middle-trigger
- ▶ Offset error:
  - ▷ Before calibration:  $\pm 60$  mV max
  - ▷ After calibration:  $\pm 1$  mV max
- ▶ Gain error (relative to calibration reference):
  - ▷ Before calibration: 0.6% of reading
  - ▷ After calibration (gain = 1):
    - 0.03% of reading max for PCI/PCIe/PXI-62204/62208
    - 0.01% of reading max for PCI/PCIe/PXI-62205/62206
  - ▷ Gain 1 with gain error adjusted to 0 at gain=1:
    - 0.05% of reading max



## Analog Output (AO)

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**NOTE** The PCI/PCIe/PXI-62208 card does not support this function.

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- ▶ Channels: Two-channel analog voltage output
- ▶ DA converter: LTC7545 or equivalent
- ▶ Max update rate: 1 MS/s
- ▶ Resolution: 12-bit
- ▶ FIFO buffer size:
  - ▷ 512 samples per channel when both channels are enabled for timed DA output
  - ▷ 1024 samples when only one channel is used for timed DA output
- ▶ Data transfers:
  - ▷ Programmed I/O
  - ▷ Bus-mastering DMA with scatter/gather
- ▶ Output range:  $\pm 10$  V, 0 V to 10 V,  $\pm$ AOEXTREF, 0 to AOEXTREF
- ▶ Settling time: 3 S to 0.5 LSB accuracy
- ▶ Slew rate: 20 V/ $\mu$ S
- ▶ Output coupling: DC
- ▶ Protection: Short-circuit to ground
- ▶ Output impedance: 0.01 $\Omega$  typical
- ▶ Output driving current:  $\pm 5$  mA max
- ▶ Stability: Any passive load, up to 1500 pF
- ▶ Power-on state: 0V steady-state
- ▶ Power-on glitch:  $\pm 1.5$  V/500  $\mu$ S
- ▶ Relative accuracy:  $\pm 0.5$  LSB typical,  $\pm 1$  LSB max
- ▶ DNL:  $\pm 0.5$  LSB typical,  $\pm 1.2$  LSB max
- ▶ Offset error:
  - ▷ Before calibration:  $\pm 80$  mV max
  - ▷ After calibration:  $\pm 1$  mV max
- ▶ Gain error:
  - ▷ Before calibration:  $\pm 0.8\%$  of output max
  - ▷ After calibration:  $\pm 0.02\%$  of output max

### **General Purpose Digital I/O (G.P. DIO, 82C55A)**

- ▶ Channels: 24 programmable input/output
- ▶ Compatibility: TTL
- ▶ Input voltage:
  - ▷ Logic Low:  $V_{IL}=0.8\text{ V}$  max;  $I_{IL}=0.2\text{ mA}$  max
  - ▷ High:  $V_{IH}=2.0\text{ V}$  max;  $I_{IH}=0.02\text{ mA}$  max
- ▶ Output voltage:
  - ▷ Low:  $V_{OL}=0.5\text{ V}$  max;  $I_{OL}=8\text{ mA}$  max
  - ▷ High:  $V_{OH}=2.7\text{ V}$  min;  $I_{OH}=400\text{ }\mu\text{A}$
- ▶ Synchronous Digital Inputs (SDI): On PCI/PCIe/PXI-62204 model only.
  - ▷ Channels: 8 digital inputs sampled simultaneously with the analog signal input
  - ▷ Compatibility: TTL/CMOS
  - ▷ Input voltage:
    - Logic Low:  $V_{IL}=0.8\text{ V}$  max;  $I_{IL}=0.2\text{ mA}$  max
    - Logic High:  $V_{IH}=2.7\text{ V}$  min;  $I_{IL}=0.02\text{ mA}$  max

### **General Purpose Timer/Counter (GPTC)**

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**NOTE**      The PCI/PCIe/PXI-62208 does not support this function.

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- ▶ Channels: 2 independent up/down timer/counters
- ▶ Resolution: 16-bit
- ▶ Compatibility: TTL
- ▶ Clock source: Internal or external
- ▶ Max source frequency: 10 MHz

### **Analog Trigger (A.Trig)**

- ▶ Source:
  - ▷ All analog input channels
  - ▷ External analog trigger (EXTATRIG)
- ▶ Level:  $\pm$ Full-scale, internal;  $\pm$ 10 V external
- ▶ Resolution: 8-bit
- ▶ Slope: Positive or negative (software-selectable)
- ▶ Hysteresis: Programmable
- ▶ Bandwidth: 400 kHz

### **External Analog Trigger Input (EXTATRIG)**

- ▶ Input Impedance:
  - ▷ 40 k $\Omega$  for PCI/PCIe/PXI-62204/62208
  - ▷ 20 k $\Omega$  for PCI/PCIe/PXI-62205/62206
- ▶ Coupling: DC
- ▶ Protection: Continuous  $\pm$ 35 V maximum

### **Digital Trigger (D.Trig)**

- ▶ Compatibility: TTL/CMOS
- ▶ Response: Rising or falling edge
- ▶ Pulse Width: 10 ns min

### **System Synchronous Interface (SSI)**

- ▶ Trigger lines: 7

### **Stability**

- ▶ Recommended warm-up time: 15 minutes
- ▶ On-board calibration reference:
  - ▷ Level: 5.000 V
  - ▷ Temperature coefficient:  $\pm$ 2 ppm/ $^{\circ}$ C
  - ▷ Long-term stability: 6 ppm/1000 Hr

## Physical

### ▶ Dimensions:

- ▷ 175mm by 107mm for PCI/PCIe62204/62205/62206/62208
- ▷ Standard CompactPCI form factor for PXI-62204/62205/62206/62208

### ▶ I/O connector: 68-pin female VHDCI type (e.g. AMP-787254-1)

## Power Requirement (typical)

### ▶ +5 VDC

- ▷ 1.3 A for PCI/PCIe/PXI-62204
- ▷ 1.2 A for PCI/PCIe/PXI-62205/62206
- ▷ 950 mA for PCI/PCIe/PXI-62208

### ▶ +12 VDC

- ▷ 358 mA for PCIe-62204
- ▷ 344 mA for PCIe-62205
- ▷ 390 mA for PCIe-62206
- ▷ 258 mA for PCIe-62208

### ▶ +3.3 VDC

- ▷ 815 mA for PCIe-62204
- ▷ 735 mA for PCIe-62205
- ▷ 710 mA for PCIe-62206
- ▷ 815 mA for PCIe-62208

## Operating Environment

- ▶ Ambient temperature: 0°C to 55°C
- ▶ Relative humidity: 10% to 90% non-condensing

## Storage Environment

- ▶ Ambient temperature: -20°C to 80°C
- ▶ Relative humidity: 5% to 95% non-condensing

## 1.4 Software Support

JYTEK provides versatile software drivers and packages for users' different approach to building up a system. JYTEK not only provides programming libraries such as DLL for most Windows-based systems, but also provide drivers for other software packages .

Contact your JYTEK to get the free SeeSharp open source software.

### Programming Library

For customers who are writing their own programs, we provide function libraries for many different operating systems, including:

D2K-DASK: Include device drivers and DLL for Windows<sup>®</sup> 7/10. DLL is binary compatible across Windows 7/10. This means all applications developed with D2K-DASK are compatible across Windows 7/10. The developing environment can be VB, VC++, Delphi, BC5, or any Windows programming language that allows calls to a DLL. The user's guide and function reference manual of D2K-DASK are on the website. ([www.jytek.com](http://www.jytek.com))

D2K-DASK/X: Include device drivers and shared library for Linux. The developing environment can be Gnu C/C++ or any programming language that allows linking to a shared library. The user's guide and function reference manual of D2K-DASK/X are on the website. ([www.jytek.com](http://www.jytek.com))

## 2 Installation

This chapter describes how to install the PCI/PCIe/PXI-62204/62205/62206/62208 card. The contents of the package and unpacking information that you should be aware of are outlined first.

The PCI/PCIe/PXI-62204/62205/62206/62208 card performs an automatic configuration of the IRQ and port address. You can use the PCI\_SCAN software utility to read the system configuration.

### 2.1 Contents of Package

In addition to this User's Manual, the package includes the following items:

- ▶ PCI/PCIe/PXI-62204/62205/62206/62208 multi-function data acquisition card

If any of these items are missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.

### 2.2 Unpacking

Your PCI/PCIe/PXI-62204/62205/62206/62208 card contains electro-static sensitive components that can be easily be damaged by static electricity.

Therefore, the card should be handled on a grounded anti-static mat. The operator should be wearing an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the card package for obvious damages. Shipping and handling may cause damage to the card. Be sure there are no shipping and handling damages on the modules carton before continuing.

After opening the card module carton, extract the system module and place it only on a grounded anti-static surface with component side up.

Again, inspect the module for damages. Press down on all the socketed IC's to make sure that they are properly seated. Do this only with the module place on a firm flat surface.

You are now ready to install your PCI/PCIe/PXI-62204/62205/62206/62208 card.

## 2.3 Card Layout

### PCIe-62204/62205/62206/62208

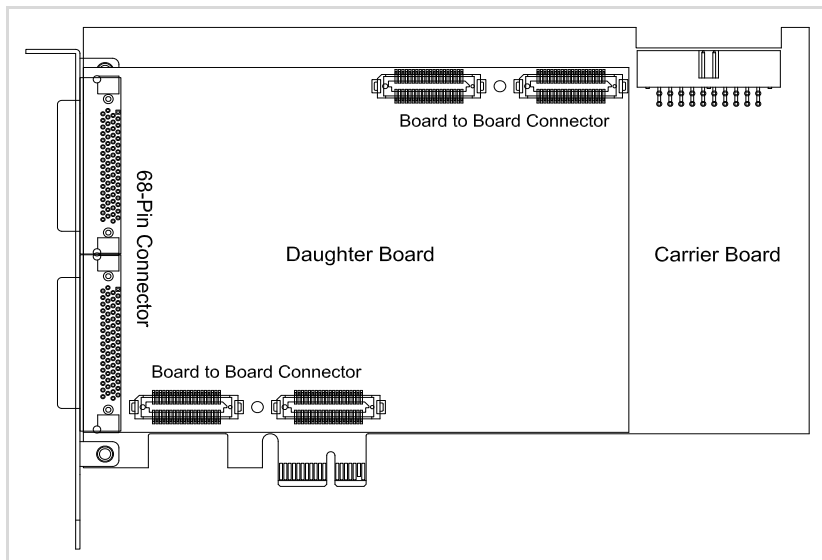


Figure 2-1: PCIe-62204/62205/62206/62208 Card Layout

### PCI-62204/62205/62206/62208

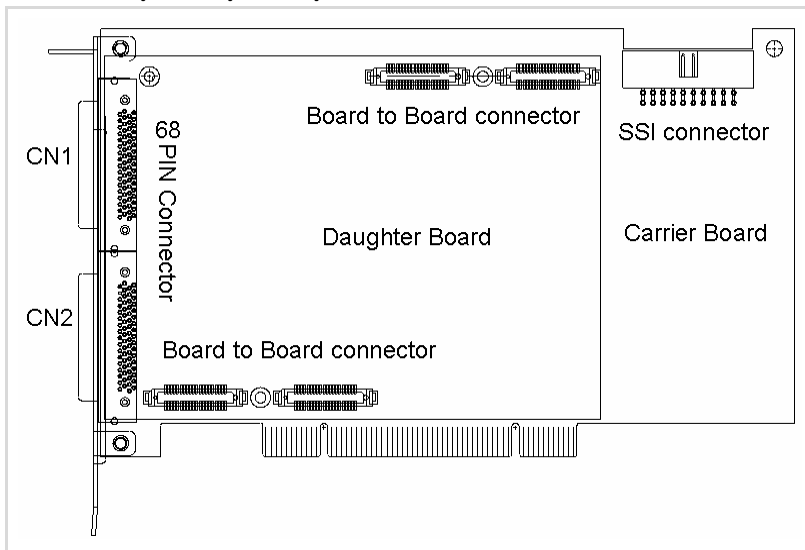


Figure 2-2: PCI-62204/62205/62206/62208 Card Layout

### PXI-62204/62205/62206/62208

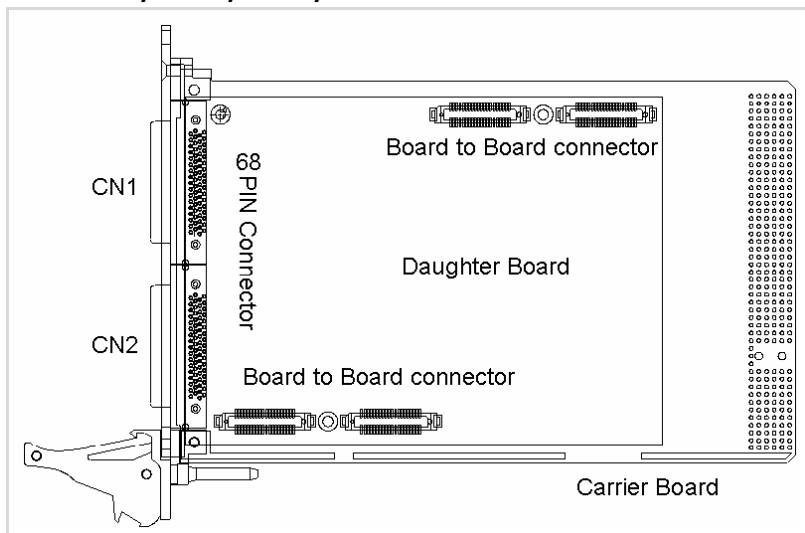


Figure 2-3: PXI-62204/62205/62206/62208 Card Layout



## 2.4 PCI Configuration

### Plug and Play

With support for plug and play, the card requests an interrupt number via its PCI controller. The system BIOS responds with an interrupt assignment based on the card information and on known system parameters. These system parameters are determined by the installed drivers and the hardware load seen by the system.

### Configuration

The board configuration is done on a board-by-board basis for all PCI boards in the system. Because configuration is controlled by the system and software, there is no jumper setting required for base address, DMA, and interrupt IRQ.

The configuration is subject to change with every boot of the system as new boards are added or removed.

### Troubleshooting

If your system doesn't boot or if you experience erratic operation with your PCI board in place, it is likely caused by an interrupt conflict. The BIOS Setup may be incorrectly configured. Consult the BIOS documentation that comes with your system to solve this problem.

## 3 Signal Connections

This chapter describes PCI/PCIe/PXI-62204/62205/62206/62208 card connectors and the signal connection between the PCI/PCIe/PXI-62204/62205/62206/62208 card and external devices.

### 3.1 Connectors Pin Assignment

The PCI/PCIe/PXI-62204/62205/62206/62208 card is equipped with two 68-pin VHDCI-type connector (AMP-787254-1). It is used for digital input/output, analog input/output, timer/counter signals, etc. One 20-pin ribbon male connector is used for SSI (System Synchronous Interface) in PCI/PCIe-62204/62205/62206/62208 card. The pin assignments of the connectors are defined in Table 3-1, Table 3-2, Table 3-3, and Table 3-4.

## CN1 Connector

AI0 (AIH0)	<b>1</b>	<b>35</b>	(AIL0) AI32
AI1 (AIH1)	<b>2</b>	<b>36</b>	(AIL1) AI33
AI2 (AIH2)	<b>3</b>	<b>37</b>	(AIL2) AI34
AI3 (AIH3)	<b>4</b>	<b>38</b>	(AIL3) AI35
AI4 (AIH4)	<b>5</b>	<b>39</b>	(AIL4) AI36
AI5 (AIH5)	<b>6</b>	<b>40</b>	(AIL5) AI37
AI6 (AIH6)	<b>7</b>	<b>41</b>	(AIL6) AI38
AI7 (AIH7)	<b>8</b>	<b>42</b>	(AIL7) AI39
AI8 (AIH8)	<b>9</b>	<b>43</b>	(AIL8) AI40
AI9 (AIH9)	<b>10</b>	<b>44</b>	(AIL9) AI41
AI10 (AIH10)	<b>11</b>	<b>45</b>	(AIL10) AI42
AI11 (AIH11)	<b>12</b>	<b>46</b>	(AIL11) AI43
AI12 (AIH12)	<b>13</b>	<b>47</b>	(AIL12) AI44
AI13 (AIH13)	<b>14</b>	<b>48</b>	(AIL13) AI45
AI14 (AIH14)	<b>15</b>	<b>49</b>	(AIL14) AI46
AI15 (AIH15)	<b>16</b>	<b>50</b>	(AIL15) AI47
AISENSE	<b>17</b>	<b>51</b>	AIGND
AI16 (AIH16)	<b>18</b>	<b>52</b>	(AIL16) AI48
AI17 (AIH17)	<b>19</b>	<b>53</b>	(AIL17) AI49
AI18 (AIH18)	<b>20</b>	<b>54</b>	(AIL18) AI50
AI19 (AIH19)	<b>21</b>	<b>55</b>	(AIL19) AI51
AI20 (AIH20)	<b>22</b>	<b>56</b>	(AIL20) AI52
AI21 (AIH21)	<b>23</b>	<b>57</b>	(AIL21) AI53
AI22 (AIH22)	<b>24</b>	<b>58</b>	(AIL22) AI54
AI23 (AIH23)	<b>25</b>	<b>59</b>	(AIL23) AI55
AI24 (AIH24)	<b>26</b>	<b>60</b>	(AIL24) AI56
AI25 (AIH25)	<b>27</b>	<b>61</b>	(AIL25) AI57
AI26 (AIH26)	<b>28</b>	<b>62</b>	(AIL26) AI58
AI27 (AIH27)	<b>29</b>	<b>63</b>	(AIL27) AI59
AI28 (AIH28)	<b>30</b>	<b>64</b>	(AIL28) AI60
AI29 (AIH29)	<b>31</b>	<b>65</b>	(AIL29) AI61
AI30 (AIH30)	<b>32</b>	<b>66</b>	(AIL30) AI62
AI31 (AIH31)	<b>33</b>	<b>67</b>	(AIL31) AI63
EXTATRIG	<b>34</b>	<b>68</b>	AIGND

**Table 3-1: CN1 Pin Assignment for PCI/PCIe/PXI-62204/62205/62206**

\* Symbols in “( )” are for differential mode connection.

AI0 (AIH0)	1	35	(AIL0) AI48
AI1 (AIH1)	2	36	(AIL1) AI49
AI2 (AIH2)	3	37	(AIL2) AI50
AI3 (AIH3)	4	38	(AIL3) AI51
AI4 (AIH4)	5	39	(AIL4) AI52
AI5 (AIH5)	6	40	(AIL5) AI53
AI6 (AIH6)	7	41	(AIL6) AI54
AI7 (AIH7)	8	42	(AIL7) AI55
AISENSE	9	43	AIGND
AI8 (AIH8)	10	44	(AIL8) AI56
AI9 (AIH9)	11	45	(AIL9) AI57
AI10 (AIH10)	12	46	(AIL10) AI58
AI11 (AIH11)	13	47	(AIL11) AI59
AI12 (AIH12)	14	48	(AIL12) AI60
AI13 (AIH13)	15	49	(AIL13) AI61
AI14 (AIH14)	16	50	(AIL14) AI62
AI15 (AIH15)	17	51	(AIL15) AI63
AI16 (AIH16)	18	52	(AIL16) AI64
AI17 (AIH17)	19	53	(AIL17) AI65
AI18 (AIH18)	20	54	(AIL18) AI66
AI19 (AIH19)	21	55	(AIL19) AI67
AI20 (AIH20)	22	56	(AIL20) AI68
AI21 (AIH21)	23	57	(AIL21) AI69
AI22 (AIH22)	24	58	(AIL22) AI70
AI23 (AIH23)	25	59	(AIL23) AI71
AIGND	26	60	AIGND
AI24 (AIH24)	27	61	(AIL24) AI72
AI25 (AIH25)	28	62	(AIL25) AI73
AI26 (AIH26)	29	63	(AIL26) AI74
AI27 (AIH27)	30	64	(AIL27) AI75
AI28 (AIH28)	31	65	(AIL28) AI76
AI29 (AIH29)	32	66	(AIL29) AI77
AI30 (AIH30)	33	67	(AIL30) AI78
AI31 (AIH31)	34	68	(AIL31) AI79

**Table 3-2: CN1 Pin Assignment for PCI/PCIe/PXI-62208**

\* Symbols in “()” are for differential mode connection.

## CN2 Connector

DA0OUT	1	35	AOGND
DA1OUT	2	36	AOGND
AOEXTREF	3	37	AOGND
NC	4	38	NC
DGND	5	39	DGND
EXTWFTRIG	6	40	DGND
EXTDTRIG	7	41	DGND
SSHOUT	8	42	SDI0 / DGND*
RESERVED	9	43	SDI1 / DGND*
RESERVED	10	44	SDI2 / DGND*
AFI1	11	45	SDI3 / DGND*
AFI0	12	46	DGND
GPTCO_SRC	13	47	DGND
GPTCO_GATE	14	48	DGND
GPTCO_UPDOWN	15	49	DGND
GPTCO_OUT	16	50	DGND
GPTC1_SRC	17	51	DGND
GPTC1_GATE	18	52	DGND
GPTC1_UPDOWN	19	53	DGND
GPTC1_OUT	20	54	DGND
EXTTIMEBASE	21	55	DGND
PB7	22	56	PB6
PB5	23	57	PB4
PB3	24	58	PB2
PB1	25	59	PB0
PC7	26	60	PC6
PC5	27	61	PC4
DGND	28	62	DGND
PC3	29	63	PC2
PC1	30	64	PC0
PA7	31	65	PA6
PA5	32	66	PA4
PA3	33	67	PA2
PA1	34	68	PA0

**Table 3-3: CN2 Pin Assignment for PCI/PCIe/PXI-62204/62205/62206**

*\*Pin 42~45 are SDI<0.3> for PCI/PCIe/PXI-62204; DGND for PCI/PCIe/PXI-62205/62206*

AI32 (AIH32)	1	35	(AIL32) AI80
AI33 (AIH33)	2	36	(AIL33) AI81
AI34 (AIH34)	3	37	(AIL34) AI82
AI35 (AIH35)	4	38	(AIL35) AI83
AI36 (AIH36)	5	39	(AIL36) AI84
AI37 (AIH37)	6	40	(AIL37) AI85
AI38 (AIH38)	7	41	(AIL38) AI86
AI39 (AIH39)	8	42	(AIL39) AI87
EXTATRIG	9	43	AIGND
AI40 (AIH40)	10	44	(AIL40) AI88
AI41 (AIH41)	11	45	(AIL41) AI89
AI42 (AIH42)	12	46	(AIL42) AI90
AI43 (AIH43)	13	47	(AIL43) AI91
AI44 (AIH44)	14	48	(AIL44) AI92
AI45 (AIH45)	15	49	(AIL45) AI93
AI46 (AIH46)	16	50	(AIL46) AI94
AI47 (AIH47)	17	51	(AIL47) AI95
AIGND	18	52	AIGND
NC	19	53	NC
EXTDTRIG	20	54	AFIO
EXTTIMEBASE	21	55	DGND
PB7	22	56	PB6
PB5	23	57	PB4
PB3	24	58	PB2
PB1	25	59	PB0
PC7	26	60	PC6
PC5	27	61	PC4
DGND	28	62	DGND
PC3	29	63	PC2
PC1	30	64	PC0
PA7	31	65	PA6
PA5	32	66	PA4
PA3	33	67	PA2
PA1	34	68	PA0

**Table 3-4: CN2 Pin Assignment for PCI/PCIe/PXI-62208**

## CN1/CN2 Connector Signal Description

Signal Name	Reference	Direction	Description
AIGND	—	—	Analog ground for AI. All three ground references (AIGND, AOGND, and DGND) are connected together on board.
AI<0..63/95>	AIGND	Input	<ul style="list-style-type: none"> <li>For PCI/PCIe/PXI-62204/62205/62206: Analog Input Channels 0~63. Each channel pair, AI&lt;i, i+32&gt; (i=0..31) can be configured either two single-ended inputs or one differential input pair (marked as AIH&lt;0..31&gt; and AIL&lt;0..31&gt;).</li> <li>For PCI/PCIe/PXI-62208: Analog Input Channels 0~95. Each channel pair, AI&lt;i, i+48&gt; (i=0..37) can be configured either two single-ended inputs or one differential input pair (marked as AIH&lt;0..47&gt; and AIL&lt;0..47&gt;).</li> </ul>
AISENSE	AIGND	Input	Analog Input Sense. This pin is the reference for any channels AI<0..63> in NRSE input configuration.
EXTATRIG	AIGND	Input	External AI analog trigger
DA0OUT	AOGND	Output	AO channel 0
DA1OUT	AOGND	Output	AO channel 1
AOEXTREF	AOGND	Input	External reference for AO channels
AOGND	—	—	Analog ground for AO
EXTWFTRIG	DGND	Input	External AO waveform trigger
EXTDTRIG	DGND	Input	External AI digital trigger
RESERVED	—	Output	Reserved. Please leave it open
SDI<0..3> <i>(for 62204 only)</i>	DGND	Input	Synchronous digital inputs. These 4 digital inputs are sampled simultaneously with the analog signal input.
GPTC<0,1>_SRC	DGND	Input	Source of GPTC<0,1>
GPTC<0,1>_GATE	DGND	Input	Gate of GPTC<0,1>

**Table 3-5: CN1/CN2 Signal Description**

Signal Name	Reference	Direction	Description
GPTC<0,1>_OUT	DGND	Input	Output of GPTC<0,1>
GPTC<0,1>_UPDOWN	DGND	Input	Up/Down of GPTC<0,1>
EXTTIMEBASE	DGND	Input	External Timebase
DGND	—	—	Digital ground
PB<7,0>	DGND	PIO*	Programmable DIO of 8255 Port B
PC<7,0>	DGND	PIO*	Programmable DIO of 8255 Port C
PA<7,0>	DGND	PIO*	Programmable DIO of 8255 Port A
AFI0	DGND	Input	Auxiliary Function Input 0 (ADCONV, AD_START)
AFI1	DGND	Input	Auxiliary Function Input 1 (DAWR, DA_START)

**Table 3-5: CN1/CN2 Signal Description**



## SSI Connector

SSI_TIMEBASE	1	2	DGND
SSI_ADCONV	3	4	DGND
SSI_DAWR / RESERVED*	5	6	DGND
SSI_SCAN_START	7	8	DGND
RESERVED	9	10	DGND
SSI_AD_TRIG	11	12	DGND
SSI_DA_TRIG / RESERVED*	13	14	DGND
RESERVED	15	16	DGND
RESERVED	17	18	DGND
RESERVED	19	20	DGND

**Table 3-6: SSI Connector Pin Assignment**

\*Pin 5 and 13 are reserved for PCI/PXI-62208.

### SSI Connector Signal Description:

SSI Timing Signal	Setting	Function
SSI_TIMEBASE	Master	Send the TIMEBASE out
	Slave	Accept the SSI_TIMEBASE to replace the internal TIMEBASE signal.
SSI_ADCONV	Master	Send the ADCONV out
	Slave	Accept the SSI_ADCONV to replace the internal ADCONV signal.
SSI_SCAN_START	Master	Send the SCAN_START out
	Slave	Accept the SSI_SCAN_START to replace the internal SCAN_START signal.
SSI_AD_TRIG	Master	Send the internal AD_TRIG out
	Slave	Accept the SSI_AD_TRIG as the digital trigger signal.
SSI_DAWR	Master	Send the DAWR out.
	Slave	Accept the SSI_DAWR to replace the internal DAWR signal.
SSI_DA_TRIG	Master	Send the DA_TRIG out.
	Slave	Accept the SSI_DA_TRIG as the digital trigger signal.

**Table 3-7: SSI Connector Legend**

## 3.2 Analog Input Signal Connection

The PCI/PCIe/PXI-62204/62205/62206/62208 card provides up to 64 single-ended or 32 differential analog input channels. You can fill the Channel Gain Queue to get desired combination of the input signal types. The analog signal can be converted to digital values by the A/D converter. To avoid ground loops and get more accurate measurements from the A/D conversion, it is important to understand the signal source type and how to connect the analog input signals.

### Types of signal sources

#### Floating Signal Sources

A floating signal source means it is not connected in any way to the buildings ground system. A device with an isolated output is a floating signal source, such as optical isolator outputs, transformer outputs, and thermocouples.

#### Ground-Referenced Signal Sources

A ground-referenced signal means it is connected in some way to the building system. That is, the signal source is already connected to a common ground point with respect to the PCI/PCIe/PXI-62204/62205/62206/62208 card, assuming that the computer is plugged into the same power system. Non-isolated outputs of instruments and devices that plug into the buildings power system are ground-referenced signal sources.

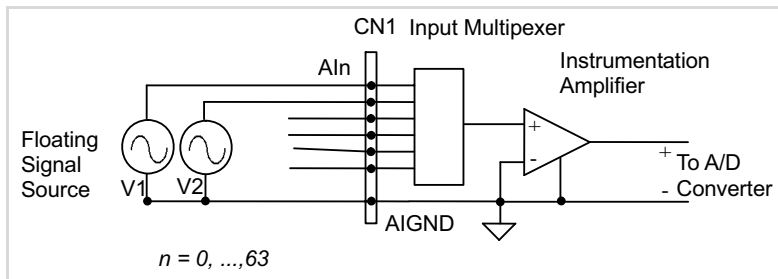
### Input Configurations

#### Single-Ended Connections

A single-ended connection is used when the analog input signal is referenced to a ground that can be shared with other analog input signals. There are two types of single-ended connections: RSE and NRSE. In RSE configuration, the PCI/PCIe/PXI-62204/62205/62206/62208 card provides the grounding point for the external analog input signals and is suitable for floating signal sources. In the NRSE configuration the board does not provide the grounding point, the external analog input signal provides its own reference grounding point and is suitable for ground-referenced signals.

Referenced Single-ended (RSE) Mode

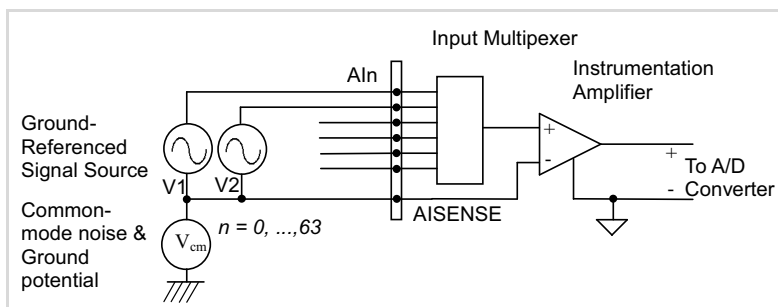
In referenced single-ended mode, all input signals are connected to the ground provided by the PCI/PCIe/PXI-62204/62205/62206/62208 card. This is suitable for connections with floating signal sources. Figure 3-1 shows an illustration. Note that when more than two floating sources are connected, these sources will be referenced to the same common ground.



**Figure 3-1: Floating Source and RSE Input Connections**

#### Non-Referenced Single-ended (NRSE) Mode

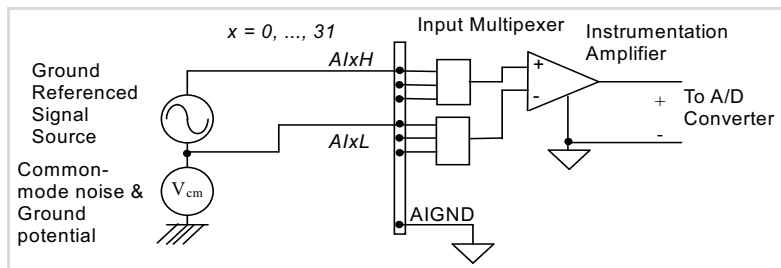
To measure ground-referenced signal sources, which are connected to the same ground point, you can connect the signals in NRSE mode. Figure 3-2 illustrates the connection. The signals local ground reference is connected to the negative input of the instrumentation Amplifier (AISENSE pin on CN1 connector), and the common-mode noise between signal ground and the ground on board will be rejected by the instrumentation amplifier.



**Figure 3-2: Ground-referenced Sources and NRSE Input Connections**

## Differential Input Mode

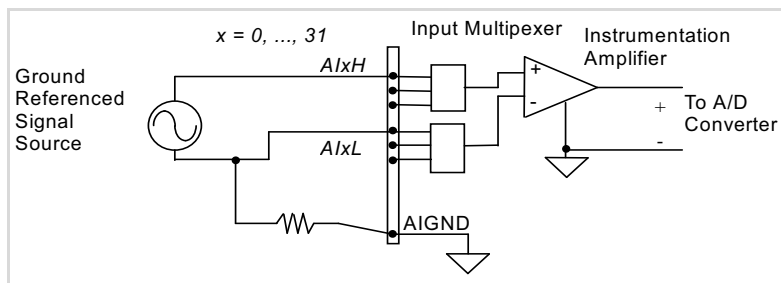
The differential input mode provides two inputs that respond to signal voltage difference between them. If the signal source is ground-referenced, the differential mode can be used for the common-mode noise rejection. Figure 3-3 shows the connection of ground-referenced signal sources under differential input mode.



**Figure 3-3: Ground-referenced Source and Differential Input**

### Ground-referenced Source and Differential Input

Figure 3-4 shows how to connect a floating signal source to the PCI/PCIe/PXI-62204/62205/62206/62208 card in differential input mode. For floating signal sources, you need to add a resistor at each channel to provide a bias return path. The resistor value should be about 100 times the equivalent source impedance. If the source impedance is less than 100ohms, you can simply connect the negative side of the signal to A1GND as well as the negative input of the Instrumentation Amplifier without any resistors. In differential input mode, less noise couples into the signal connections than in single-ended mode.



**Figure 3-4: Floating Source and Differential Input**

## 4 Operation Theory

The operation theory of the PCI/PCIe/PXI-62204/62205/62206/62208 card functions are described in this chapter. The functions include the A/D conversion, D/A conversion, digital I/O, and general purpose counter/timer. The operation theory can help you understand how to configure and program the PCI/PCIe/PXI-62204/62205/62206/62208 card.

### 4.1 A/D Conversion

When using an A/D converter, you must know about the properties of the signal to be measured. You may decide which channel to use and how to connect the signals to the card. In addition, users should define and control the A/D signal configurations, including channels, gains, and polarities (unipolar/bipolar).

The A/D acquisition is initiated by a trigger source and you must decide how to trigger the A/D conversion. The data acquisition will start once a trigger condition is matched.

After the end of an A/D conversion, the A/D data is buffered in a Data FIFO. The A/D data can now be transferred into the system memory for further processing.

#### PCI/PCIe/PXI-62204/62208 AI Data Format

##### Synchronous Digital Inputs (PCI/PCIe/PXI-62204 only)

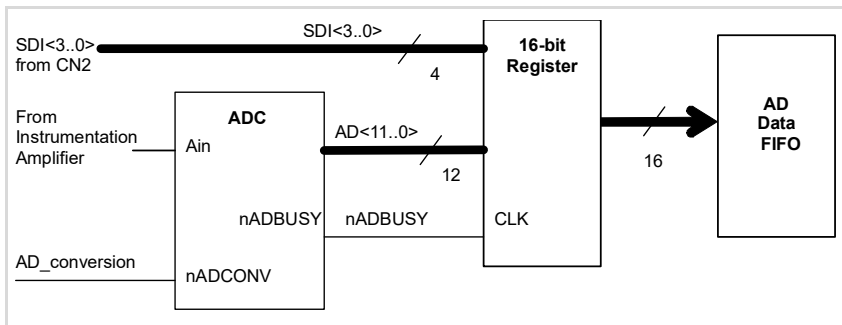
When each A/D conversion is completed, the 14-bits converted digital data accompanied with 2 bits of SDI<1..0>\_X per channel from J5 will be latched into the 16-bit register and data FIFO as shown in Figure 4-1 and Figure 4-2. Therefore, you can simultaneously sample one analog signal with four digital signals. The data format of every acquired 16-bit data is as follows:

D11, D10, D9 ..... D1, D0, b3, b2, b1, b0

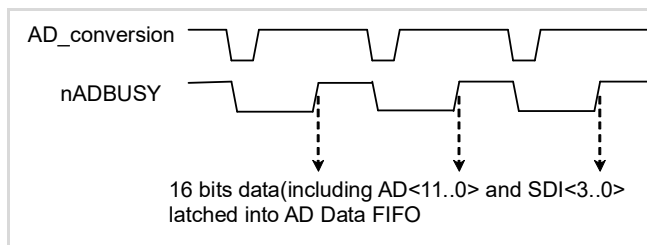
Where

D11, D10, D9 ..... D1, D0: 2's complement A/D 12-bit data

b3, b2, b1, b0: Synchronous Digital Inputs SDI<3..0>



**Figure 4-1: Synchronous Digital Inputs Block Diagram**



**Figure 4-2: Synchronous Digital Inputs Timing**

**NOTE**

Since the analog signal is sampled when an A/D conversion starts (falling edge of A/D\_conversion signal), while SDI<3..0> are sampled right after an A/D conversion completes (rising edge of nADBUSHY signal). Precisely SDI<3..0> are sampled with 280ns lag to the analog signal.

Table 4-1 and Table 4-2 illustrate the ideal transfer characteristics of various input ranges of the PCI/PCIe/PXI-62204/62205/62206/62208 card.

Description	Bipolar Analog Input Range				Digital code
Full-scale Range	±10V	±5V	±2.5V	±1.25V	—
Least significant bit	4.88mV	2.44mV	1.22mV	0.61mV	—
FSR-1LSB	9.9951V	4.9976V	2.4988V	1.2494V	7FFX
Midscale +1LSB	4.88mV	2.44mV	1.22mV	0.61mV	001X
Midscale	0V	0V	0V	0V	000X
Midscale -1LSB	-4.88mV	-2.44mV	-1.22mV	-0.61mV	FFFX
-FSR	-10V	-5V	-2.5V	-1.25V	800X

**Table 4-1: Bipolar Analog Input Range and Output Digital Code on PCI/PCIe/PXI-62204/62208**

*Note that the last 4 digital codes are SDI<3..0> and is supported only on PCI/PCIe/PXI-62204)*

Description	Unipolar Analog Input Range			Digital code
Full-scale Range	0V to 10V	0 to +5V	0 to +2.5V	—
Least significant bit	2.44mV	1.22mV	0.61mV	—
FSR-1LSB	9.9976V	4.9988V	2.9994V	7FFX
Midscale +1LSB	5.00244V	2.50122V	1.25061V	001X
Midscale	5V	2.5V	1.25V	000X
Midscale -1LSB	4.9976V	2.4988V	1.2494V	FFFX
-FSR	0V	0V	0V	800X

**Table 4-2: Unipolar Analog Input Range and Output Digital Code on PCI/PCIe/PXI-62204/62208**

*Note that the last 4 digital codes are SDI<3..0> and is supported only on PCI/PCIe/PXI-62204.*

## PCI/PCIe/PXI-62205/62206 AI Data Format

The data format of the acquired 16-bit A/D data is **2's Complement coding**. Table 4-3 and Table 4-4 illustrate the valid input ranges and the ideal transfer characteristics.

Description	Bipolar Analog Input Range				Digital code
Full-scale Range	±10V	±5V	±2.5V	±1.25V	—
Least significant bit	305.2 $\mu$ V	152.6 $\mu$ V	76.3 $\mu$ V	38.15 $\mu$ V	—
FSR-1LSB	9.999695V	4.999847V	2.499924V	1.249962V	7FFF
Midscale +1LSB	305.2 $\mu$ V	152.6 $\mu$ V	76.3 $\mu$ V	38.15 $\mu$ V	0001
Midscale	0V	0V	0V	0V	0000
Midscale -1LSB	-305.2 $\mu$ V	-152.6 $\mu$ V	-76.3 $\mu$ V	-38.15 $\mu$ V	FFFF
-FSR	-10V	-5V	-2.5V	-1.25V	8000

**Table 4-3: Bipolar Analog Input Range and Output Digital Code for PCI/PCIe/PXI-62205/62206**

Description	Unipolar Analog Input Range				Digital code
Full-scale Range	0V to 10V	0 to +5V	0 to +2.5V	0 to +1.25V	—
Least significant bit	152.6 $\mu$ V	76.3 $\mu$ V	38.15 $\mu$ V	19.07 $\mu$ V	—
FSR-1LSB	9.999847V	4.999924V	2.499962V	1.249981V	7FFF
Midscale +1LSB	5.000153V	2.500076V	1.250038V	0.625019V	0001
Midscale	5V	2.5V	1.25V	0.625V	0000
Midscale -1LSB	4.999847V	2.499924V	1.249962V	0.624981V	FFFF

**Table 4-4: Unipolar Analog Input Range and Output Digital Code for PCI/PCIe/PXI-62205/62206**



## Software Conversion with Polling Data Transfer Acquisition Mode (Software Polling)

This is the easiest way to acquire a single A/D data. The A/D converter starts one conversion whenever the dedicated software command is executed. Then the software would poll the conversion status and read the A/D data back when it is available.

This method is very suitable for applications that needs to process A/D data in real time. Under this mode, the timing of the A/D conversion is fully controlled by the software. However, it is difficult to control the A/D conversion rate.

### Specifying Channel, Gain, and Input Configurations in the Channel Gain Queue

In Software Polling and Programmable Scan Acquisition mode, the channel, gain, polarity, and input configuration (RSE, NRSE, or DIFF) can be specified in the Channel Gain Queue. You can fill the channel number in the Channel Gain Queue in any order. The channel order of acquisition will be the same as the order you set in the Channel Gain Queue. Therefore, you can acquire data with user-defined channel orders and with different settings on each channel.

When the specified channels have been sampled from the first data to the last data in the Channel Gain Queue, the settings in Channel Gain Queue are maintained. You do not need to re-configure the Channel Gain Queue if you want to keep on sampling data in the same order. The maximum number of entries you can set in the Channel Gain Queue is 512.

Example:

First you can set entries in Channel Gain Queue:

- ▶ Ch3 with bipolar  $\pm 10V$ , RSE connection
- ▶ Ch1 with bipolar  $\pm 2.5V$ , DIFF connection
- ▶ Ch2 with unipolar 5V, NRSE connection
- ▶ Ch1 with bipolar  $\pm 2.5V$ , DIFF connection

If you read 10 data by software polling method, then the acquisition sequence of channels is 3, 1, 2, 1, 3, 1, 2, 1, 3, 1.

## Programmable Scan Acquisition Mode

### Scan Timing and Procedure

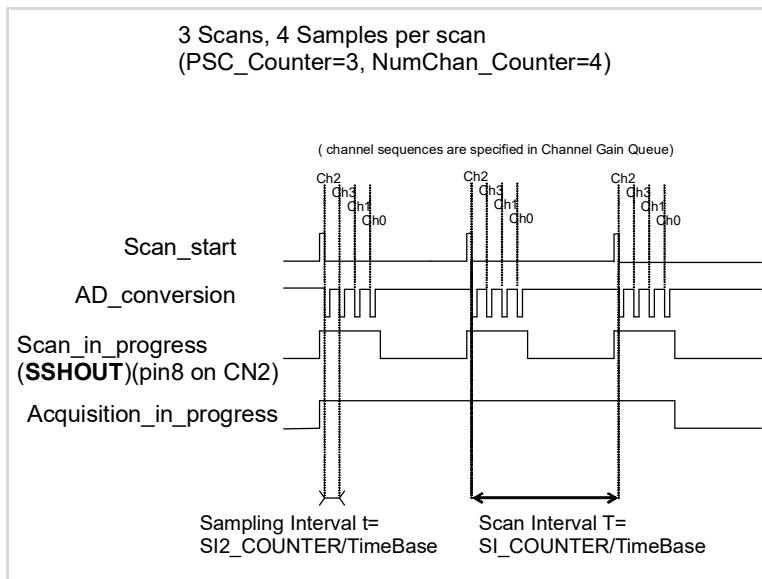
It is recommended that you use this mode if your applications need a fixed and precise A/D sampling rate. You can accurately program the period between conversions of individual channels. There are at least four counters which need to be specified:

- ▶ SI\_counter (24-bit): Specify the Scan Interval =  $SI\_counter / \text{Timebase}$
- ▶ SI2\_counter (16-bit): Specify the data Sampling Interval =  $SI2\_counter / \text{Timebase}$
- ▶ PSC\_counter (24-bit): Specify Post Scan Counts after a trigger event
- ▶ NumChan\_counter (9-bit): Specify the number of samples per scan

The acquisition timing and the meanings of the 2 counters are illustrated in Figure 4-3.

### TIMEBASE Clock Source

In scan acquisition mode, all the A/D conversions start on the output of counters, which use TIMEBASE as the clock source. By software you can specify the TIMEBASE to be either an internal clock source (onboard 40 MHz clock) or an external clock input (EXTTIMEBASE) on CN2 connector. The external TIMEBASE is useful when you want to acquire data at rates not available with the internal A/D sample clock. The external clock source should generate TTL-compatible continuous clocks and with a maximum frequency of 40 MHz while the minimum should be 1 MHz. Refer to section 4.6 for information on user-controllable timing signals.



**Figure 4-3: Scan Timing**

There are four trigger modes to start the scan acquisition. Refer to section 4.1 for details. The data transfer mode is discussed in the following section.

**NOTES**

The maximum A/D sampling rate is 3 MHz for PCI/PCIe/PXI-62204/62208, 500 kHz for PCI/PCIe/PXI-62205, and 250 kHz for PCI/PCIe/PXI-62206. Therefore, the minimum setting of SI2\_counter is 14 for PCI/PCIe/PXI-62204/62208, 80 for PCI/PCIe/PXI-62205, and 160 for PCI/PCIe/PXI-62206 while using the internal TIMEBASE.

The SI\_counter is a 24-bit counter and the SI2\_counter is a 16-bit counter. The maximum scan interval using the internal Timebase =  $224/40$  Ms = 0.419 s, and the maximum sampling interval between two channels using the internal Timebase =  $216/40$  Ms = 1.638 ms.

The scan interval may not be smaller than the product of the data sampling interval and the NumChan\_counter value. The relationship can be represented as:  $SI\_counter \geq SI2\_counter * NumChan\_counter$ .

### Scan with SSH

You can send the SSHOUT signal on CN2 to external S&H circuits to sample and hold all signals if you want to simultaneously sample all channels in a scan, as illustrated in Figure 4-3.

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**NOTES**      The PCI/PCIe/PXI-62208 does not support this function.

The SSHOUT signal is sent to external S&H circuits to hold the analog signal. You must implement external S&H circuits on their own to carry out the S&H function. There are no onboard S&H circuits.

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### Specifying Channels, Gains, and Input Configurations in the Channel Gain Queue

Like software polling acquisition mode, the channel, gain, and input configurations can be specified in the Channel Gain Queue under the scan acquisition mode. Note that in scan acquisition mode, the number of entries in the Channel Gain Queue is normally equivalent to the value of NumChan\_counter (that is, the number of samples per scan).

Example: Set

- ▶ SI2\_counter = 160
- ▶ SI\_counter = 640
- ▶ PSC\_counter = 3
- ▶ NumChan\_counter = 4
- ▶ Timebase = Internal clock source
- ▶ Channel entries in the Channel Gain Queue: ch1, ch2, ch0, ch2

Then

- ▶ Acquisition sequence of channels: 1, 2, 0, 2, 1, 2, 0, 2, 1, 2, 0, 2
- ▶ Sampling interval:  $160/40 \text{ Ms} = 4 \mu\text{s}$
- ▶ Scan interval:  $640/40 \text{ Ms} = 16 \mu\text{s}$
- ▶ Equivalent sampling rate of ch0, ch1: 62.5 kHz
- ▶ Equivalent sampling rate of ch2: 125 kHz

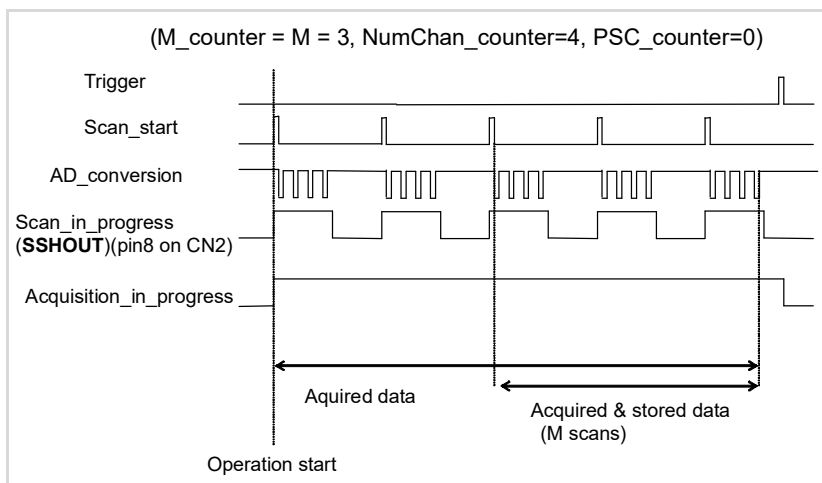
## Trigger Modes

The PCI/PCIe/PXI-62204/62205/62206/62208 card provides four trigger sources (internal software trigger, external analog trigger, and digital trigger sources, and SSI trigger signals). You must select one of them as the source of the trigger event. A trigger event occurs when the specified condition is detected on the selected trigger source. For example, a rising edge on the external digital trigger input. Refer to section 4.6 for more information on SSI signals.

There are four trigger modes (pre-trigger, post-trigger, middle-trigger, and delay-trigger) working with the four trigger sources to initiate different scan data acquisition timing when a trigger event occurs. They are described in the following sections. For information on trigger sources, refer to section 4.5.

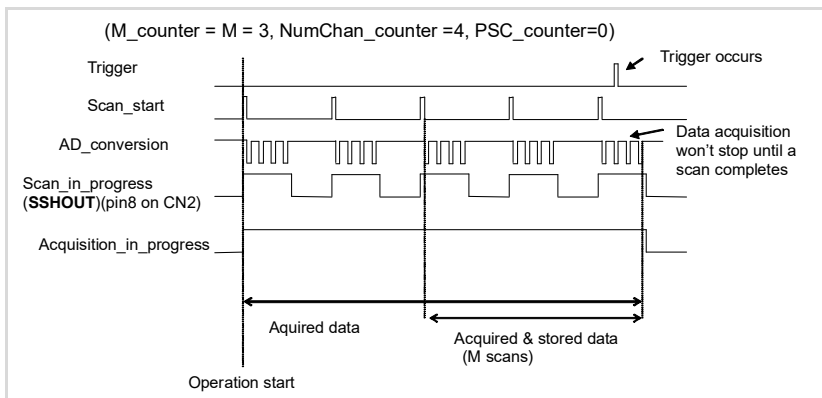
## Pre-Trigger Acquisition

Use pre-trigger acquisition in applications where you want to collect data before a trigger event. The A/D starts to sample when you execute the specified function calls to begin the pre-trigger operation, and it stops when the trigger event occurs. Users must program the value  $M$  in  $M\_counter$  (16 bits) to specify the amount of the stored scans before the trigger event. If an external trigger occurs, the program only stores the last  $M$  scans of data converted before the trigger event, as illustrated in Figure 4-4, where  $M\_counter = M = 3$ ,  $PSC\_counter = 0$ . The post scan count is 0 because there is no sampling after the trigger event in pre-trigger acquisition. The total stored amount of data = Number of enabled channels \*  $M\_counter$ .



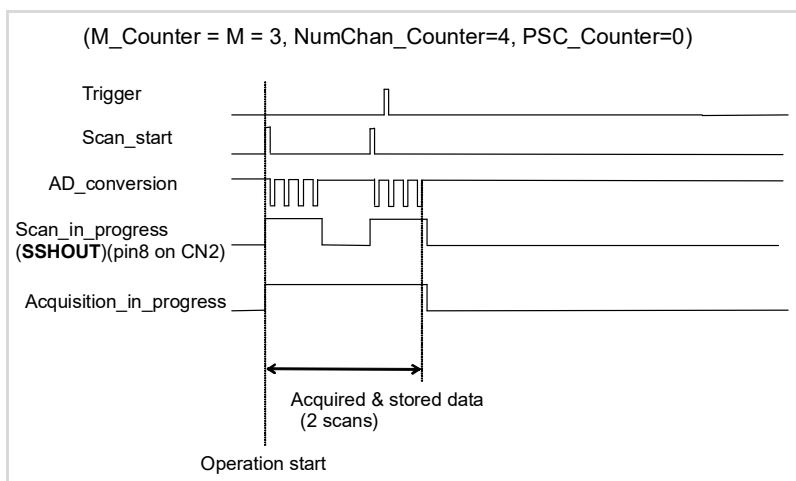
**Figure 4-4: Pre-trigger (Trigger occurs after M scans)**

Note that if a trigger event occurs when a scan is in progress, the data acquisition won't stop until the scan completes, and the stored M scans of data includes the last scan. Therefore, the first stored data will always be the first channel entry of a scan (that is, the first channel entry in the Channel Gain Queue if the number of entries in the Channel Gain Queue is equivalent to the value of NumChan\_counter), no matter when a trigger signal occurs, as illustrated in Figure 16, where  $M\_counter = M = 3$ ,  $NumChan\_counter = 4$ ,  $PSC\_counter = 0$ .



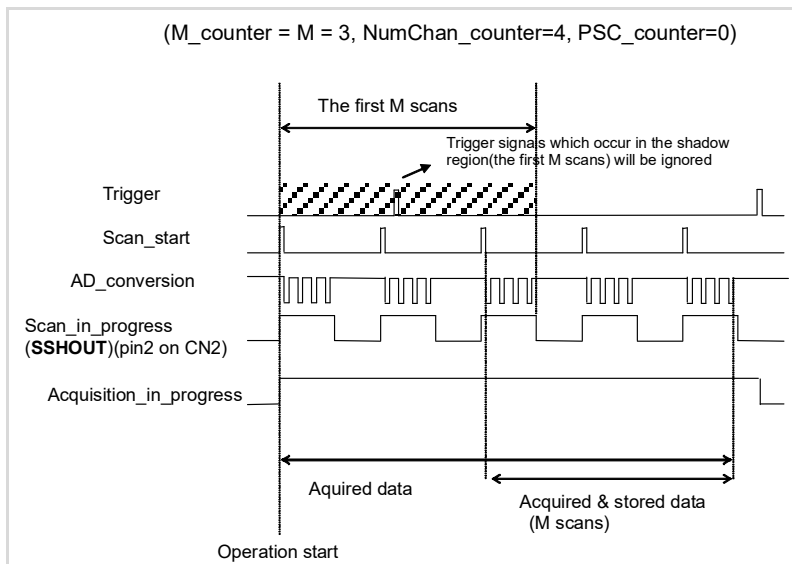
**Figure 4-5: Pre-trigger (Trigger with scan in progress)**

When the trigger signal occurs before the first M scans of data are converted, the amount of stored data could be fewer than the originally specified amount M\_counter, as illustrated in Figure 4-6. This situation can be avoided by setting M\_enable. If M\_enable is set to 1, the trigger signal will be ignored until the first M scans of data are converted, and it assures the user M scans of data under pre-trigger mode, as illustrated in Figure 4-7. However, if M\_enable is set to 0, the trigger signal will be accepted any time, as shown in Figure 4-6. Note that the total amount of stored data will always be equal to the number in the M\_counter because data acquisition does not stop until a scan is completed.



**Figure 4-6: Pre-trigger with M\_enable=0 (Trigger occurs before M scans)**





**Figure 4-7: Pre-trigger with M\_enable=1**

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**NOTE** The PSC\_counter is set to 0 in pre-trigger acquisition mode.

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## Middle-Trigger Acquisition

Use middle-trigger acquisition in applications where you want to collect data before and after a trigger event. The number of scans ( $M$ ) stored before the trigger is specified in  $M\_counter$ , while the number of scans ( $N$ ) after the trigger is specified in  $PSC\_counter$ .

Like pre-trigger mode, the number of stored data could be less than the specified amount of data ( $M+N$ ), if an external trigger occurs before  $M$  scans of data are converted. The  $M\_enable$  bit in middle-trigger mode takes the same effect as in pre-trigger mode. If  $M\_enable$  is set to 1, the trigger signal will be ignored until the first  $M$  scans of data are converted, and it assures the user with  $(M+N)$  scans of data under middle-trigger mode. However, if  $M\_enable$  is set to 0, the trigger signal will be accepted at any time. Figure 4-8 shows the acquisition timing with  $M\_enable=1$ .

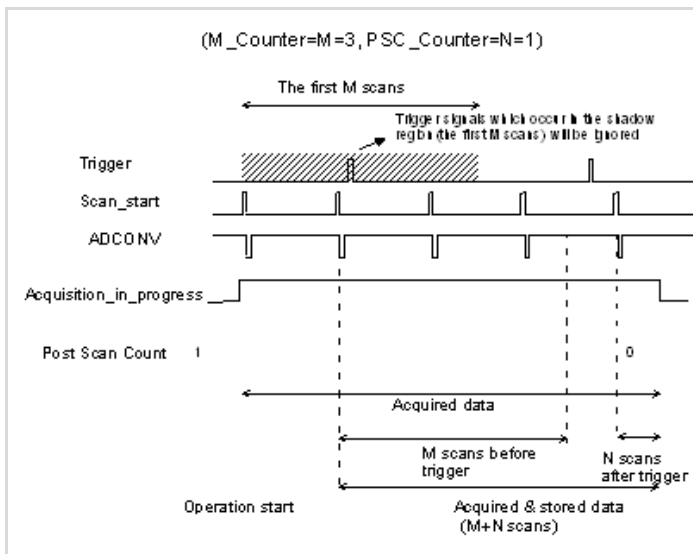
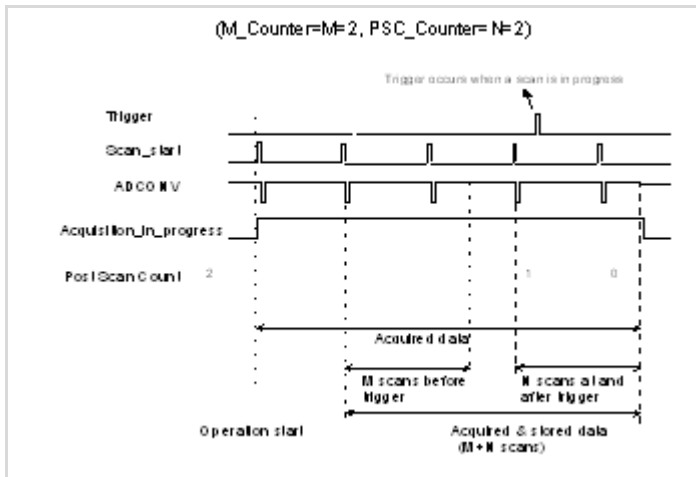


Figure 4-8: Middle-Trigger with  $M\_enable = 1$

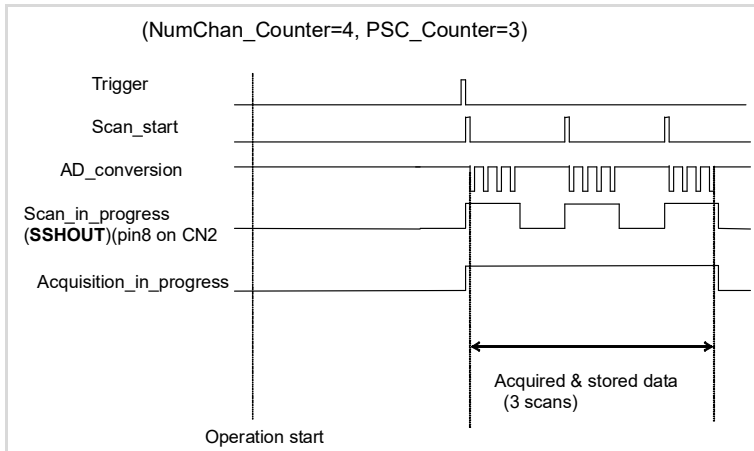
If the trigger event occurs when a scan is in progress, the stored N scans of data would include this scan, as illustrated in Figure 4-9.



**Figure 4-9: Middle-Trigger (Trigger occurs when a scan is in progress)**

## Post-Trigger Acquisition

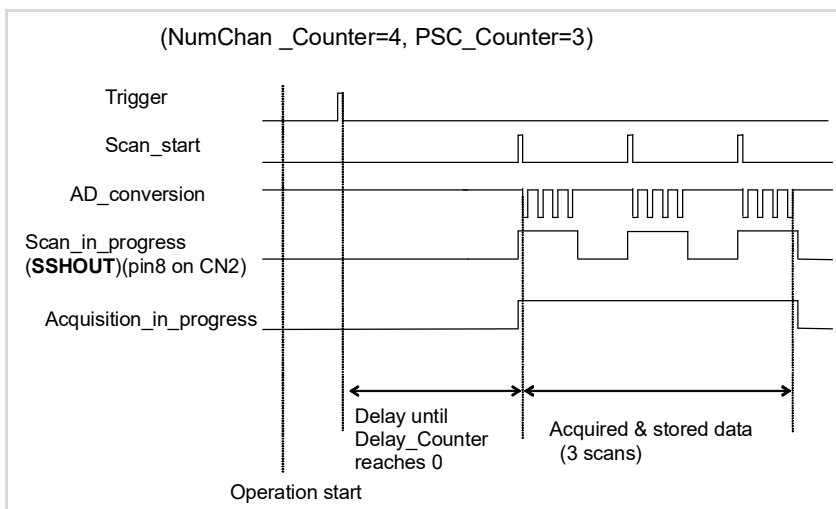
Use post-trigger acquisition in applications where you want to collect data after a trigger event. The number of scans after the trigger is specified in `PSC_counter`, as illustrated in Figure 4-10. The total acquired data length = `NumChan_counter * PSC_counter`.



**Figure 4-10: Post-trigger**

## Delay Trigger Acquisition

Use delay trigger acquisition in applications where you want to delay the data collection after the occurrence of a specified trigger event. The delay time is controlled by the value, which is pre-loaded in the Delay\_counter (16-bit). The counter counts down on the rising edge of the Delay\_counter clock source after the trigger condition is met. The clock source can be software-programmed either by the TIMEBASE clock (40 MHz) or A/D sampling clock (TIMEBASE / SI2\_counter). When the count reaches 0, the counter stops and the card starts to acquire data. The total acquired data length = NumChan\_counter \* PSC\_counter.



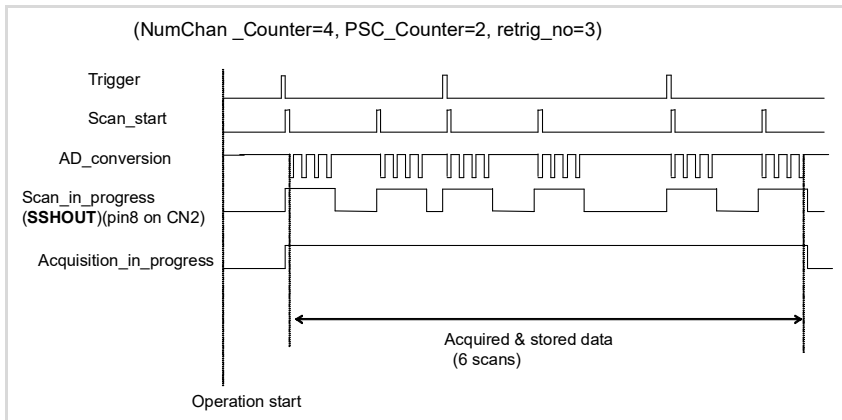
**Figure 4-11: Delay trigger**

### NOTE

When the Delay\_counter clock source is set to TIMEBASE, the maximum delay time is  $2^{16}/40$  Ms or 1.638 ms. When the source is set to A/D sampling clock, the maximum delay time may be higher than  $2^{16} * SI2\_counter / 40M$ .

### Post-Trigger or Delay-trigger Acquisition with re-trigger

Use post-trigger or delay-trigger acquisition with re-trigger function in applications where you want to collect data after several trigger events. The number of scans after each trigger is specified in PSC\_counter, and users could program Retrig\_no to specify the re-trigger numbers. Figure 4-12 illustrates an example. In this example, two scans of data is acquired after the first trigger signal, then the card waits for the re-trigger signal (re-trigger signals which occur before the first two scans is completed will be ignored). When the re-trigger signal occurs, two more scans are performed. The process repeats until specified amount of re-trigger signals are detected. The total acquired data length = NumChan\_counter \* PSC\_counter \* Retrig\_no.



**Figure 4-12: Post trigger with Re-trigger**

## Bus-mastering DMA Data Transfer

PCI bus-mastering DMA is necessary for high speed DAQ in order to utilize the maximum PCI bandwidth. The bus-mastering controller, which is built in the PLX IOP-480 PCI controller, controls the PCI bus when it becomes the master of the bus. Bus mastering reduces the size of the on-board memory and reduces the CPU loading because data is directly transferred to the computer's memory without host CPU intervention.

Bus-mastering DMA provides the fastest data transfer rate on PCI-bus. Once the analog input operation starts, control returns to your program. The hardware temporarily stores the acquired data in the onboard AD Data FIFO and then transfers the data to a user-defined DMA buffer memory in the computer. Note that even when the acquired data length is less than the Data FIFO, the AD data is not kept in the Data FIFO but directly transferred into host memory by the bus-mastering DMA.

The DMA transfer mode is complicated to program. We recommend using a high-level program library to configure this card. If users would like to know more about software programs that can handle the DMA bus master data transfer, visit to <http://www.plxtech.com> for more information on PCI controllers.

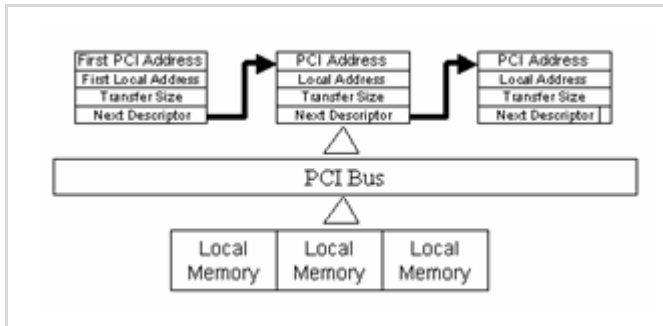
By using a high-level programming library for high speed DMA data acquisition, you simply need to assign the sampling period and the number of conversion into your specified counters. After the AD trigger condition is matched, the data is transferred to the system memory by the bus-mastering DMA.

The PCI controller also supports the function of scatter/gather bus mastering DMA, which helps you transfer large amounts of data by linking all the memory blocks into a continuous linked list.

In a multi-user or multi-tasking OS, like Windows, Linux, etc, it is difficult to allocate a large continuous memory block to do the DMA transfer. Therefore, the PLX IOP-480 provides the function of scatter/gather or chaining mode DMA to link the non-continuous memory blocks into a linked list so that you can transfer very large amounts of data without being limited by the fragment of small size memory. You can configure the linked list for the input DMA channel or the output DMA channel.

Figure 4-13 shows a linked list that is constructed by three DMA descriptors. Each descriptor contains a PCI address, a local address, a transfer size, and the pointer to the next descriptor. You can allocate many small

size memory blocks and chain their associative DMA descriptors altogether by their application programs. The PCI/PCIe/PXI-62204/62205/62206/62208 card software driver provides simple settings for the scatter/gather function, including some sample programs in the JYTEK All-in-One CD.



**Figure 4-13: Scatter/gather DMA for Data Transfer**

In non-chaining mode, the maximum DMA data transfer size is 2 M double words (8M bytes). However, there is no limitation on the DMA data transfer size when using scatter/gather chaining mode. You can also link the descriptor nodes circularly to achieve a multi-buffered mode DMA.



## 4.2 D/A Conversion

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**NOTE** The PCI/PCIe/PXI-62208 card does not support this function.

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There are two 12-bit D/A output channels available in the PCI/PCIe/PXI-62204/62205/62206 card. When using D/A converters, you should assign and control the D/A converter reference sources for the D/A operation mode and D/A channels. You could also set the output polarity to unipolar or bipolar.

The reference selection control lets you utilize in full the multiplying characteristics of the D/A converters. Internal 10V reference and external reference inputs are available in the PCI/PCIe/PXI-62204/62205/62206 card. The range of the D/A output is directly related to the reference. The digital codes that are updated to the D/A converters will multiply with the reference to generate the analog output. While using internal 10V reference, the full range would be  $-10V$  to  $+9.9951V$  in the bipolar output mode, and  $0V$  to  $9.9976V$  in the unipolar output mode. While using an external reference, you can reach different output ranges by connecting different references. For example, if connecting a DC  $-5V$  with the external reference, then you can get a full range from  $-4.9976V$  to  $+5V$  in the bipolar output with inverting characteristics due to the negative reference voltage. You could also have an amplitude modulated (AM) output by feeding a sinusoidal signal into the reference input. The range of the external reference should be within  $\pm 10V$ . Table 4-5 and Table 4-6 illustrates the relationship between digital code and output voltages with  $V_{ref}=10V$  and if internal reference is selected.

Digital Code	Analog Output
111111111111	$V_{ref} * (2047/2048)$
100000000001	$V_{ref} * (1/2048)$
100000000000	$0V$
011111111111	$-V_{ref} * (1/2048)$
000000000000	$-V_{ref}$

**Table 4-5: Bipolar Output Code Table**

Digital Code	Analog Output
111111111111	$V_{ref} * (4095/4096)$
100000000000	$V_{ref} * (2048/4096)$
000000000001	$V_{ref} * (1/4096)$
000000000000	0V

**Table 4-6: Unipolar Output Code Table**

The D/A conversion is initiated by a trigger source. You must decide how to trigger the D/A conversion. The data output will start when a trigger condition is met. Before the start of D/A conversion, D/A data is transferred from the computer's main memory to a buffering Data FIFO.

Two D/A conversion modes are available: Software Update and Timed Waveform Generation. These are described below, including the timing, trigger source control, trigger modes, and data transfer methods. Either mode may be applied to D/A channels independently. You can simultaneously software update DA CH0 while generating timed waveforms on CH1.

## Software Update

This is the easiest way to generate D/A output. To do this:

1. Specify the D/A output channels.
2. Set output polarity (unipolar or bipolar) and reference source (internal 10V or external AOEXTREF).
3. Update the digital values into D/A data registers through a software output command.

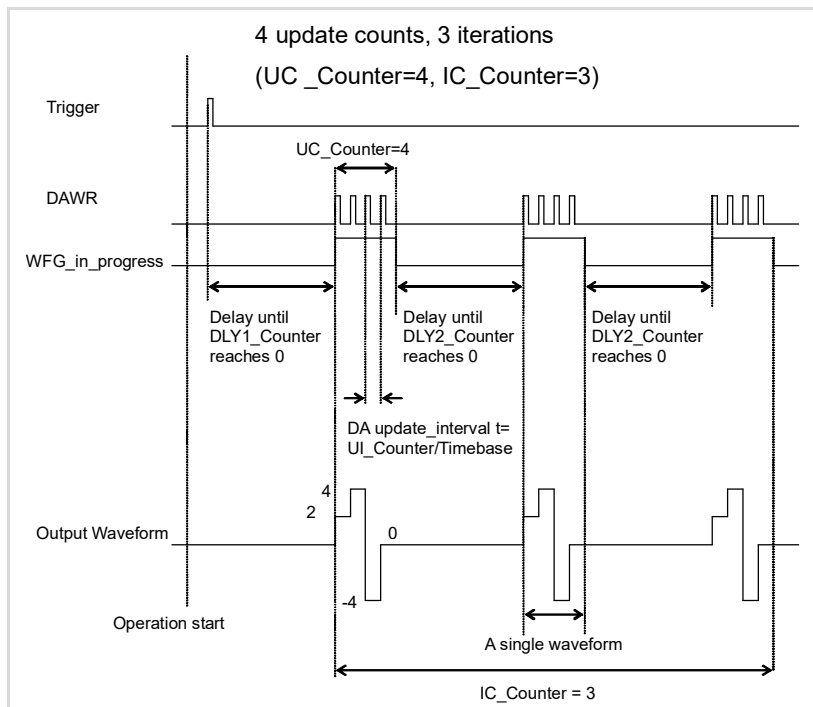
## Timed Waveform Generation

This mode can provide your applications with a precise D/A output with a fixed update rate. It can be used to generate an infinite or finite waveform. You can accurately program the update period of the D/A converters.

The D/A output timing is provided through a combination of counters in the FPGA on board. There are a total of five counters to be specified. These counters include:

- ▶ UI\_counter (24 bits): specify the DA update interval is equal to CHUI\_counter/TIMEBASE
- ▶ UC\_counter (24 bits): specify the total update counts in a single waveform
- ▶ IC\_counter (24 bits): specify the iteration counts of waveform
- ▶ DA\_DLY1\_counter (16 bits): specify the delay from the trigger to the first update start
- ▶ DA\_DLY2\_counter (16 bits): specify the delay between two consecutive waveform generations

Figure 4-14 shows a typical D/A timing diagram assuming the data in the data buffer are 2V, 4V, -4V, 0V. D/A updates its output on each rising edge of DAWR. The meaning of the counters enumerated above are discussed in the following sections.



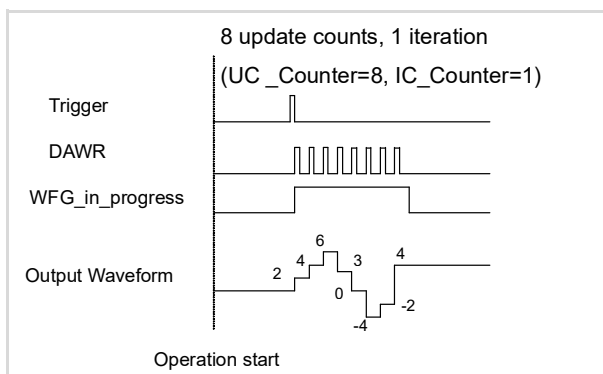
**Figure 4-14: Typical D/A Timing of Waveform Generation**

**NOTE** The maximum D/A update rate is 1 MHz. Therefore, the minimum setting of the UI\_counter is 40 while using an internal TIMEBASE (40 MHz).

## Trigger Modes

### Post-Trigger Generation

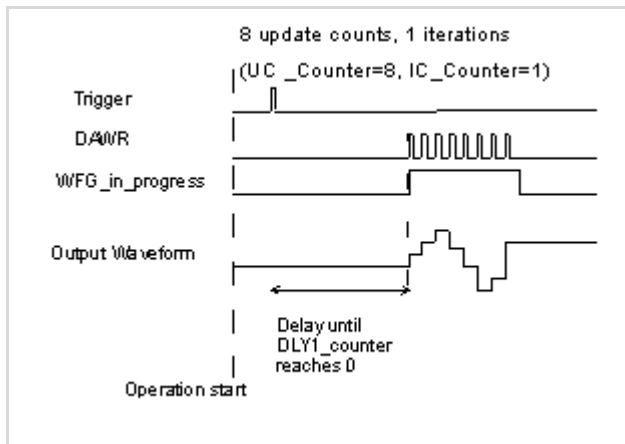
Use post-trigger when you want to perform DA waveform right after a trigger event occurs. In this trigger mode DLY1\_Counter is ignored and not be specified. Figure 4-15 shows a single waveform generated right after a trigger signal is detected and assuming the data in the data buffer are 2V, 4V, 6V, 3V, 0V, -4V, -2V, and 4V. The trigger signal could come from a software command, an analog trigger or a digital trigger. Refer to section 4.5 for detailed information.



**Figure 4-15: Post Trigger Waveform Generation**

### Delay-Trigger Generation

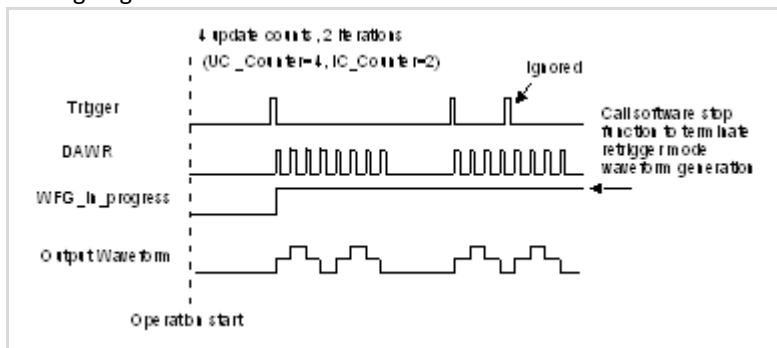
Use delay trigger when you want to delay the waveform generation after a trigger event. In Table 4-16, DA\_DLY1\_counter determines the delay time from the trigger signal to the start of the waveform generation, assuming the data in the data buffer are 2V, 4V, 6V, 3V, 0V, -4V, -2V, and 4V. DLY1\_counter counts down on the rising edge of its clock source after the trigger condition is met. When the count reaches 0, the counter stops and the PCI/PCIe/PXI-62204/62205/62206/62208 card starts the waveform generation. This DLY1\_Counter is 16-bit wide and you can set the delay time in units of TIMEBASE (delay time = DLY1\_Counter/TIMEBASE) or in units of update period (delay time = DLY1\_Counter \* UI\_counter/TIMEBASE), so the delay time can reach a wider range.



**Figure 4-16: Delay Trigger Waveform Generation**

### Post-Trigger or Delay-Trigger with Re-trigger

Use post-trigger or delay-trigger with re-trigger function when you want to generate waveform after more than one trigger events. The re-trigger function can be enabled or disabled by software setting. In Figure 4-17, each trigger signal will initiate a waveform generation assuming the data in the data buffer are 2V, 4V, 2V, and 0V. However, the trigger event would be ignored while the waveform generation is ongoing.



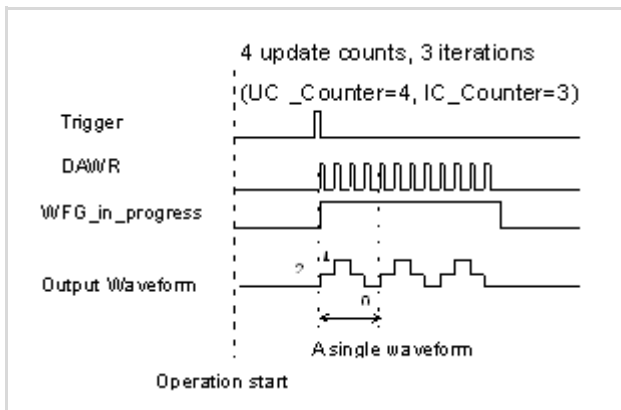
**Figure 4-17: Re-triggered Waveform Generation with Post-Trigger (DLY2\_Counter=0)**

## Iterative Waveform Generation

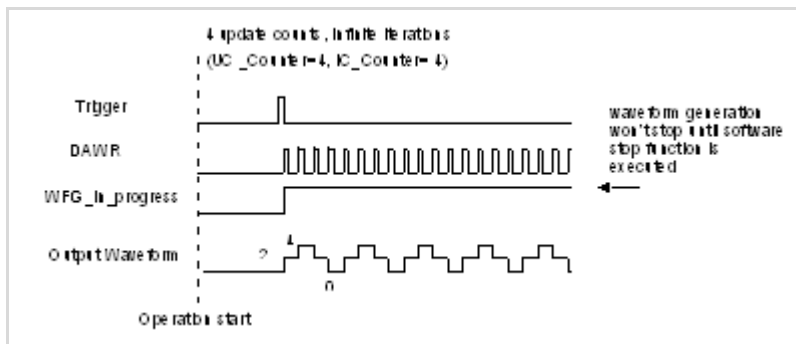
Set IC\_Counter in order to generate iterative waveforms from the data of a single waveform. The counter stores the iteration number and the iterations may be finite (Figure 4-18) or infinite (Figure 4-19). Take note that in infinite mode the waveform generation does not stop until software stop function is executed and IC\_Counter is still valid when stop mode III is selected. Both figures assume that the data in the data buffer are 2V, 4V, 2V, and 0V.

An onboard data FIFO is used to buffer the digital data for DA output. If the data size of a single waveform you specified (That is, Update Counts in UC\_counter) is less than the FIFO size, after initially transferring the data from the host PC memory to the FIFO on board, the data in the FIFO will be automatically re-transmitted whenever a single waveform is completed. Therefore, it does not occupy the PCI bandwidth when repetitive waveforms are performed. However, if the size of a single waveform were larger than that of the FIFO, it needs to be intermittently loaded from the host PC's memory via DMA, when a repetitive waveforms is performed thus PCI bandwidth would be occupied.

The data FIFO size on the PCI/PCIe/PXI-62204/62205/62206/62208 card is 1024 (words) when one DA channel is enabled, or 512 (words) when both DA channels are enabled.



**Figure 4-18: Finite Iterative Waveform Generation with Post-trigger (DLY2\_Counter = 0)**



**Figure 4-19: Infinite Iterative Waveform Generation with Post-trigger (DLY2\_Counter = 0)**

### Delay2 in Iterative Waveform Generation

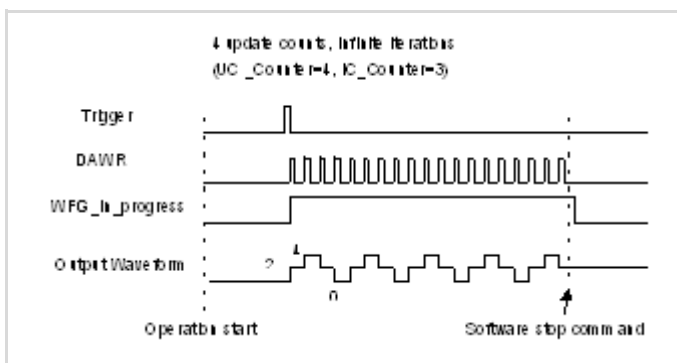
To stretch out the flexibility of the D/A waveform generation, we add a DLY2\_Counter to separate two consecutive waveforms in iterative waveform generation. The time between two waveforms is assigned by setting the value of the DLY2\_Counter. The DLY2\_Counter starts to count down after a waveform generation finishes and the next waveform generation starts right after it counts down to zero, as shown in Figure 4-20. This DLY2\_Counter is 16-bit wide and you may set the delay time in unit of TIMEBASE (delay time = DLY2\_Counter/TIMEBASE) or in unit of update period (delay time = DLY2\_Counter \* UI\_Counter/TIMEBASE), so the delay time can reach a wider range.



## Stop Modes of Scan Update

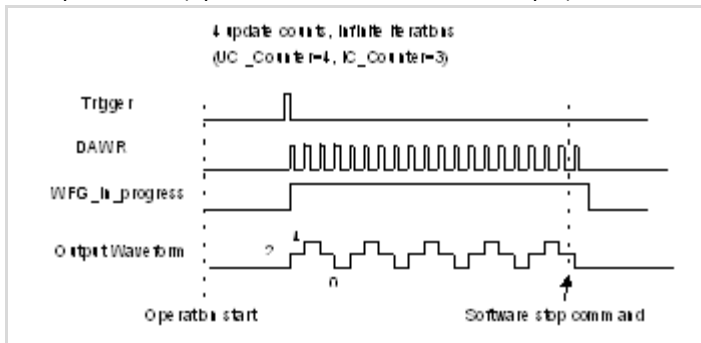
You can call software stop function to stop waveform generation when it is still in progress. Three stop modes are provided for timed waveform generation meant to stop the waveform generation. You can apply these three modes to stop waveform generation no matter infinite or finite waveform generation mode is selected.

Figure 4-20 illustrates an example for stop mode I, assuming the data in the data buffer are 2V, 4V, 2V, and 0V. In this mode, the waveform stops immediately when software command is asserted.



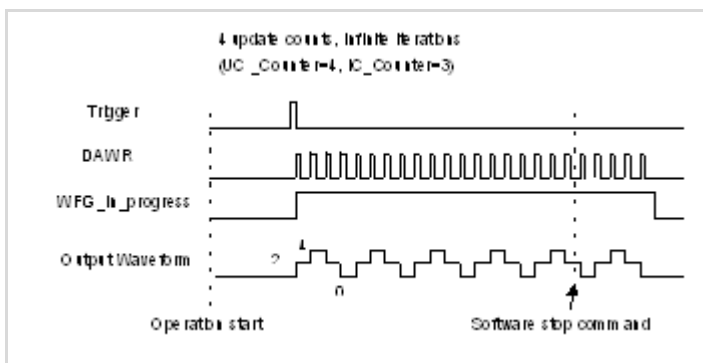
**Figure 4-20: Stop Mode I**

In stop mode II, after a software stop command is given, the waveform generation does not stop until a complete single waveform is finished. See Figure 4-21. Since the UC\_counter is set to four, the total DA update counts (number of pulses of DAWR signal) must be a multiple of four (update counts = 20 in this example).



**Figure 4-21: Stop Mode II**

In stop mode III, after a software stop command is given, the waveform generation does not stop until the performed number of waveforms is a multiple of the IC\_Counter. See Figure 4-22. Since the IC\_Counter is set to three, the total generated waveforms must be a multiple of three (waveforms = 6 in this example), and the total DA update counts must be a multiple of 12 (UC\_counter \* IC\_Counter). You can compare these three figures to see the differences.



**Figure 4-22: Stop Mode III**

### 4.3 Digital I/O

The PCI/PCIe/PXI-62204/62205/62206/62208 card contains 24 lines of general-purpose digital I/O (GPIO) which is provided through the 82C55A chip.

The 24-line GPIO are separated into three ports: Port A, Port B and Port C. Port A and Port B can be programmed to be either input or output ports. Port C can be separated into high bit (PC4-PC7) and low bit (PC0-PC3), and both high bit and low bit ports can be programmed for input or output. Upon system startup or reset, all the GPIO pins are reset to high impedance inputs.

The PCI/PCIe/PXI-2010 also provides two digital inputs per channel (SDI from CN2), which are sampled simultaneously with an analog signal input and is stored with the 12-bit AD data. Refer to Figure 4.1 for the more details.

### 4.4 General Purpose Timer/Counter Operation

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**NOTE** The PCI/PCIe/PXI-62208 card does not support this function.

---

Two independent 16-bit up/down timer/counter are designed within FPGA for various applications. They have the following features:

- ▶ Count up/down controlled by hardware or software
- ▶ Programmable counter clock source (internal or external clock up to 10 MHz)
- ▶ Programmable gate selection (hardware or software control)
- ▶ Programmable input and output signal polarities (high active or low active)
- ▶ Initial count can be loaded from software
- ▶ Current count value can be read-back by software without affecting circuit operation

## The Basics of Timer/Counter Functions

Each timer/counter has three inputs that can be controlled via hardware or software. These are clock input (GPTC\_CLK), gate input (GPTC\_GATE), and up/down control input (GPTC\_UPDOWN). The GPTC\_CLK input provides a clock source input to the timer/counter. Active edges on the GPTC\_CLK input make the counter increment or decrement. The GPTC\_UPDOWN input controls whether the counter counts up or down. The GPTC\_GATE input is a control signal which acts as a counter enable or a counter trigger signal under different applications.

The output of timer/counter is GPTC\_OUT. After power-up, GPTC\_OUT is pulled high by a pulled-up resistor about 10K ohms. Then GPTC\_OUT goes low after the PCI/PCIe/PXI-62204/62205/62206/62208 card is initialized.

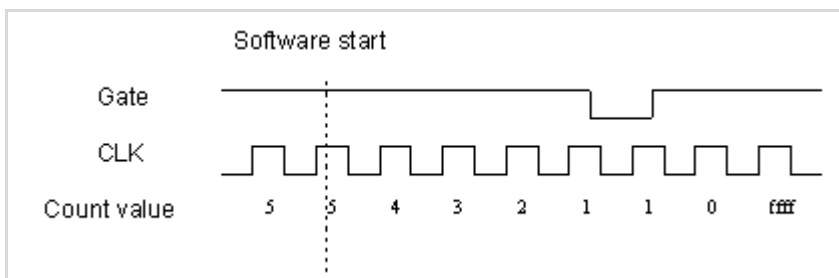
All the polarities of input/output signals can be programmed by software. In this chapter, for easy explanation, all GPTC\_CLK, GPTC\_GATE, and GPTC\_OUT are assumed to be active high or rising-edge triggered in the figures.

## General Purpose Timer/Counter modes

Eight programmable timer/counter modes are provided. All modes start operating following a software-start signal that is set by the software. The GPTC software reset initializes the status of the counter and re-loads the initial value to the counter. The operation remains halted until the software-start is re-executed. The operating theories under different modes are described in the following sections.

### Mode1: Simple Gated-Event Counting

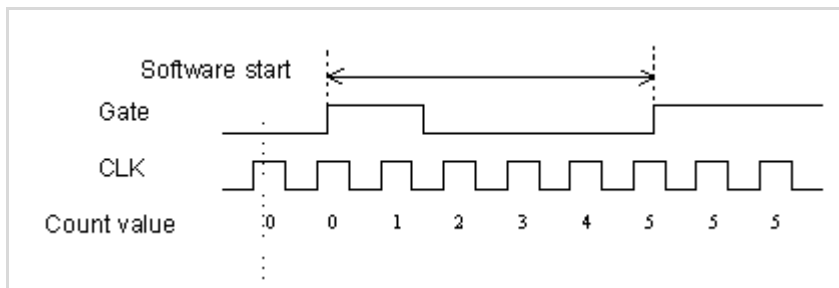
In this mode, the counter counts the number of pulses on the GPTC\_CLK after the software-start. Initial count can be loaded from software. Current count value can be read-back by software any time without affecting the counting. GPTC\_GATE is used to enable/disable counting. When GPTC\_GATE is inactive, the counter halts the current count value. Figure 4-23 illustrates the operation with initial count = 5, countdown mode.



**Figure 4-23: Mode1 Operation**

### Mode2: Single Period Measurement

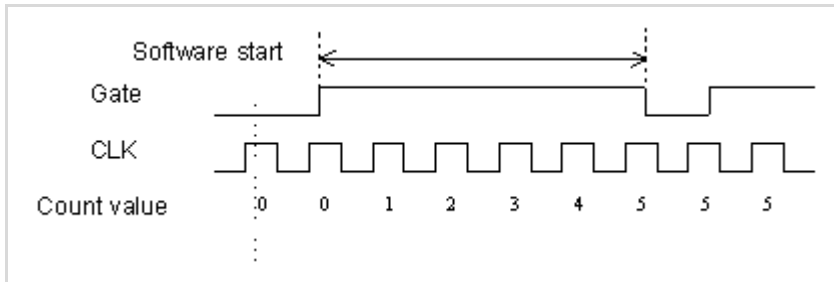
In this mode, the counter counts the period of the signal on GPTC\_GATE in terms of GPTC\_CLK. Initial count can be loaded from software. After the software-start, the counter counts the number of active edges on GPTC\_CLK between two active edges of GPTC\_GATE. After the completion of the period interval on GPTC\_GATE, GPTC\_OUT outputs high and then current count value can be read-back by software. Figure 4-24 illustrates the operation where initial count = 0, count-up mode.



**Figure 4-24: Mode2 Operation**

**Mode3: Single Pulse-width Measurement**

In this mode, the counter counts the pulse-width of the signal on GPTC\_GATE in terms of GPTC\_CLK. Initial count can be loaded from software. After the software-start, the counter counts the number of active edges on GPTC\_CLK when GPTC\_GATE is in its active state. After the completion of the pulse-width interval on GPTC\_GATE, GPTC\_OUT outputs high, then current count value can be read-back by software. Figure 4-25 illustrates the operation where initial count = 0, count-up mode.



**Figure 4-25: Mode3 Operation**

### Mode4: Single Gated Pulse Generation

This mode generates a single pulse with programmable delay and programmable pulse-width following the software-start. The two programmable parameters could be specified in terms of periods of the GPTC\_CLK input by software. GPTC\_GATE is used to enable/disable counting. When GPTC\_GATE is inactive, the counter halts the current count value. Figure 4-26 illustrates the generation of a single pulse with a pulse delay of two and a pulse-width of four.

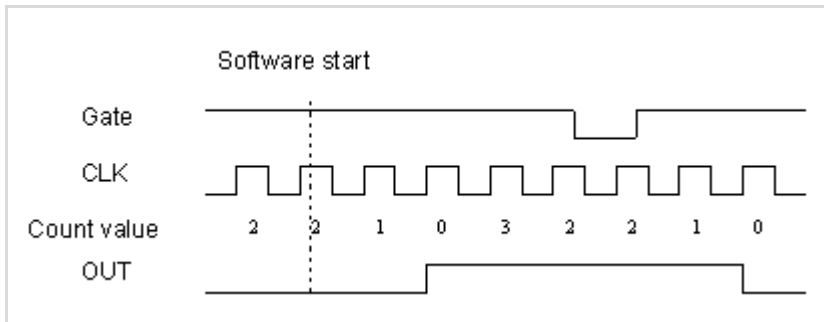
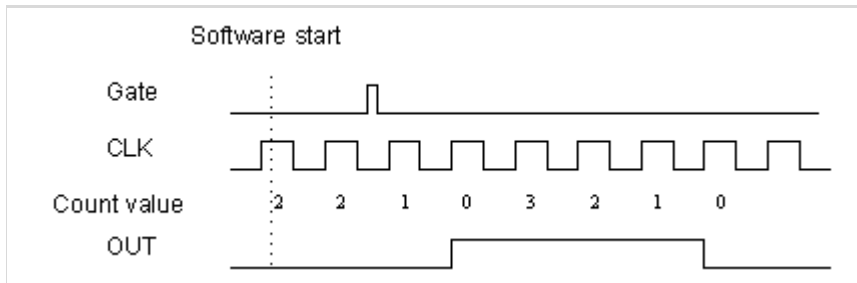


Figure 4-26: Mode4 Operation

### Mode5: Single Triggered Pulse Generation

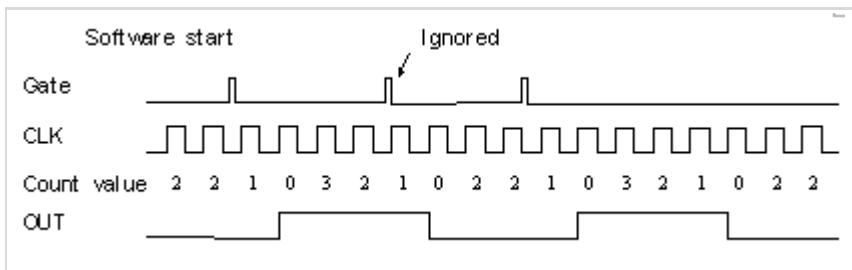
This function generates a single pulse with programmable delay and pro-grammable pulse-width following an active GPTC\_GATE edge. You could specify these programmable parameters in terms of periods of the GPTC\_CLK input. Once the first GPTC\_GATE edge triggers the single pulse, GPTC\_GATE takes no effect until the software-start is re-executed. Figure 4-27 illustrates the generation of a single pulse with a pulse delay of two and a pulse-width of four.



**Figure 4-27: Mode5 Operation**

**Mode6: Re-triggered Single Pulse Generation**

This mode is similar to Mode5 except that the counter generates a pulse following every active edge of GPTC\_GATE. After the software-start, every active GPTC\_GATE edge triggers a single pulse with programmable delay and pulse-width. Any GPTC\_GATE triggers that occur when the prior pulse is not completed would be ignored. Figure 4-28 illustrates the generation of two pulses with a pulse delay of two and a pulse-width of four.



**Figure 4-28: Mode6 Operation**



### Mode7: Single Triggered Continuous Pulse Generation

This mode is similar to Mode5 except that the counter generates continuous periodic pulses with programmable pulse interval and pulse-width following the first active edge of GPTC\_GATE. Once the first GPTC\_GATE edge triggers the counter, GPTC\_GATE takes no effect until the software-start is re-executed. Figure 4-29 illustrates the generation of two pulses with a pulse delay of four and a pulse-width of three.

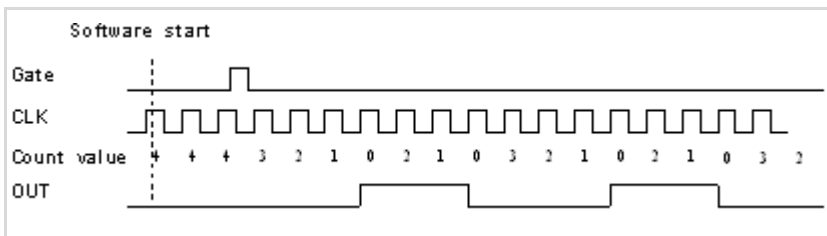


Figure 4-29: Mode7 Operation

### Mode8: Continuous Gated Pulse Generation

This mode generates periodic pulses with programmable pulse interval and pulse-width following the software-start. GPTC\_GATE is used to enable/disable counting. When GPTC\_GATE is inactive, the counter halts the current count value. Figure 4-30 illustrates the generation of two pulses with a pulse delay of four and a pulse-width of three.

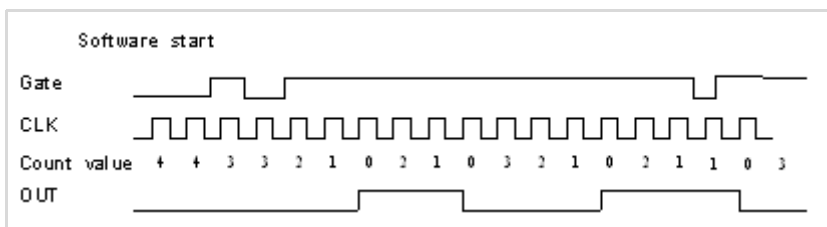


Figure 4-30: Mode8 Operation

## 4.5 Trigger Sources

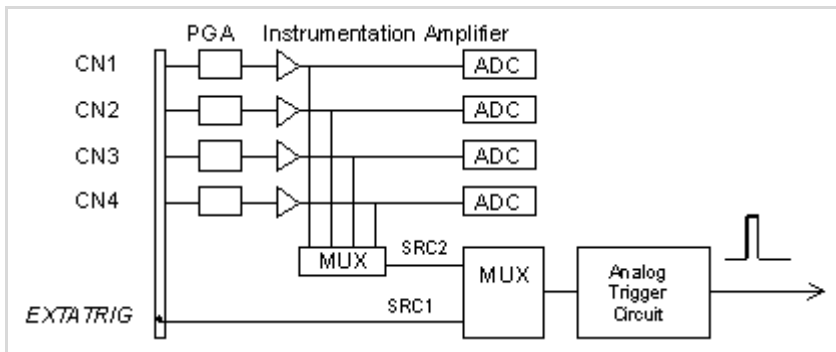
JYTEK provides flexible trigger selections in the PCI/PCIe/PXI-62204/62205/62206/62208 card. In addition to the internal software trigger, the PCI/PCIe/PXI-62204/62205/62206/62208 card also supports external analog, digital triggers, and SSI triggers. You can configure the trigger source by software for A/D and D/A processes individually. Note that the A/D and the D/A conversion share the same analog trigger.

### Software-Trigger

This trigger mode does not need any external trigger source. The trigger asserts right after you execute the specified function calls to begin the operation. A/D and D/A processes can receive an individual software trigger.

### External Analog Trigger

The analog trigger circuitry routing is shown in the Figure 4-31. The analog multiplexer can select either a direct analog input from the EXTATRIG pin (SRC1 in Figure 4-31) in the 68-pin connector or the input signal of ADC (SRC2 in Figure 4-31). That is, one of the four channel inputs you can select as a trigger source. Both trigger sources can be used for all trigger modes. The range of trigger level for SRC1 is  $\pm 10\text{V}$  and the resolution is 78mV (refer to Table 4-6), while the trigger range of SRC2 is the full-scale range of the selected channel input and the resolution is the desired range divided by 256. For example, if the channel input selected to be the trigger source is set bipolar and  $\pm 5\text{V}$  range, the trigger voltage would be 4.96V when the trigger level code is set to 0xFF while -4.96V when the code is set to 0x01.



**Figure 4-31: Analog Trigger Block Diagram**

Trigger level digital setting	Trigger voltage
0xFF	9.92V
0xFE	9.84V
0x81	0.08V
0x80	0
0x7F	-0.08V
0x01	-9.92V

**Table 4-7: Analog Trigger SRC1 (EXTATRIG) Ideal Transfer Characteristic**

The trigger signal is generated when the analog trigger condition is satisfied. There are five analog trigger conditions in the PCI/PCIe/PXI-62204/62205/62206/62208 card. The PCI/PCIe/PXI-62204/62205/62206/62208 card uses two threshold voltages, Low\_Threshold and High\_Threshold to build the five different trigger conditions. You can configure the trigger conditions easily by software.

### Below-Low Analog Trigger Condition

Figure 4-32 shows the below-low analog trigger condition, the trigger signal is generated when the input analog signal is less than the Low\_Threshold voltage, and the High\_Threshold setting is not used in this trigger condition.

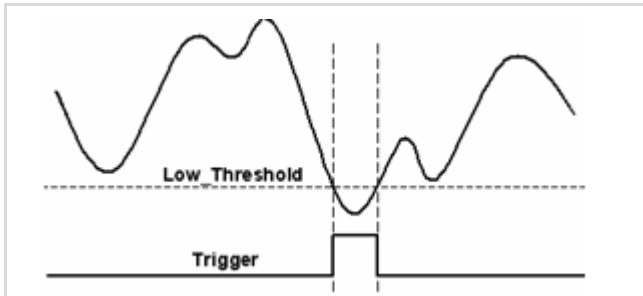


Figure 4-32: Below-Low Analog Trigger Condition

### Above-High Analog Trigger Condition

Figure 4-33 shows the above-high analog trigger condition, the trigger signal is generated when the input analog signal is higher than the High\_Threshold voltage, and the Low\_Threshold setting is not used in this trigger condition.

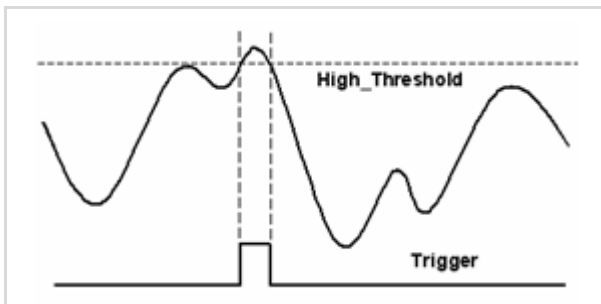


Figure 4-33: Above-High Analog Trigger Condition

### Inside-Region Analog Trigger Condition

Figure 4-34 shows the inside-region analog trigger condition, the trigger signal is generated when the input analog signal level falls in the range between the High\_Threshold and the Low\_Threshold voltages.

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**NOTE** The High\_Threshold setting should be always higher than the Low\_Threshold voltage setting.

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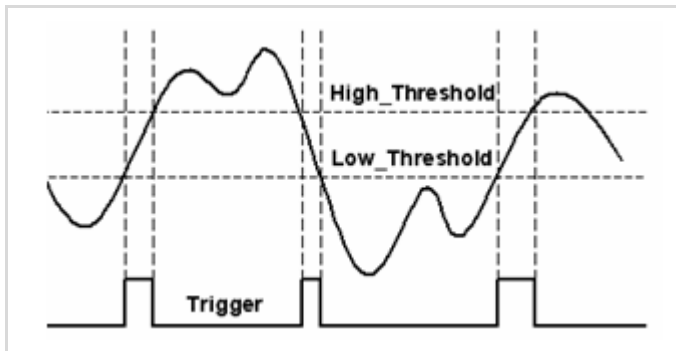
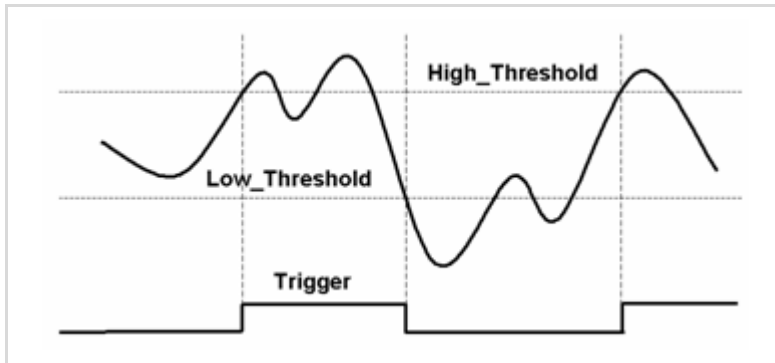


Figure 4-34: Inside-Region Analog Trigger Condition

### High-Hysteresis Analog Trigger Condition

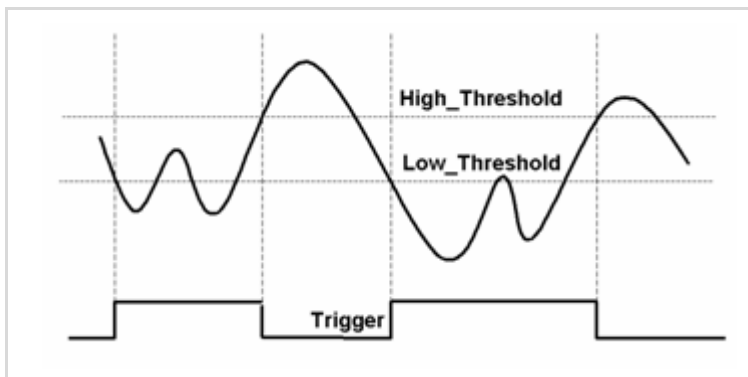
Figure 4-35 shows the high-hysteresis analog trigger condition, the trigger signal is generated when the input analog signal level is greater than the High\_Threshold voltage, and the Low\_Threshold voltage determines the hysteresis duration. Note the High\_Threshold setting should be always higher than the Low\_Threshold voltage setting.



**Figure 4-35: High-Hysteresis Analog Trigger Condition**

### Low-Hysteresis Analog Trigger Condition

Figure 4-36 shows the low-hysteresis analog trigger condition, the trigger signal is generated when the input analog signal level is less than the Low\_Threshold voltage, and the High\_Threshold voltage determines the hysteresis duration. Note the High\_Threshold setting should be always higher than the Low\_Threshold voltage setting.



**Figure 4-36: Low-Hysteresis Analog Trigger Condition**

## External Digital Trigger

An external digital trigger occurs when a rising edge or a falling edge is detected on the digital signal connected to the EXTDRIG or the EXTWFTRG of the 68-pin connector for external digital trigger. The EXTDRIG is dedicated for A/D process, and the EXTWFTRG is used for D/A process. You can program the trigger polarity using the software drivers. Note that the signal level of the external digital trigger signals should be TTL-compatible and the minimum pulse is 20 ns.



Figure 4-37: External Digital Trigger

## 4.6 User-controllable Timing Signals

In order to meet the requirements for user-specific timing and requirements for synchronizing multiple cards, the PCI/PCIe/PXI-62204/62205/62206/62208 card provides flexible user-controllable timing signals to connect to external circuitry or additional cards.

The whole DAQ timing of the PCI/PCIe/PXI-62204/62205/62206/62208 card is composed of a bunch of counters and trigger signals in the FPGA. These timing signals are related to the A/D, D/A conversions, and Timer/Counter applications. These timing signals can be input to or output from the I/O connectors, SSI connector, and the PXI bus. Therefore, the internal timing signals can be used to control external devices or circuitry. Note that in other models of PCI/PCIe/PXI-62204/62205/62206/62208 card, the user-controllable timing signals may vary. However, the SSI/PXI timing signals remain the same for every PCI/PCIe/PXI-62204/62205/62206/62208 card.

We implemented signal multiplexers in the FPGA to individually choose the desired timing signals for the DAQ operations, as shown in the Figure 4-38.

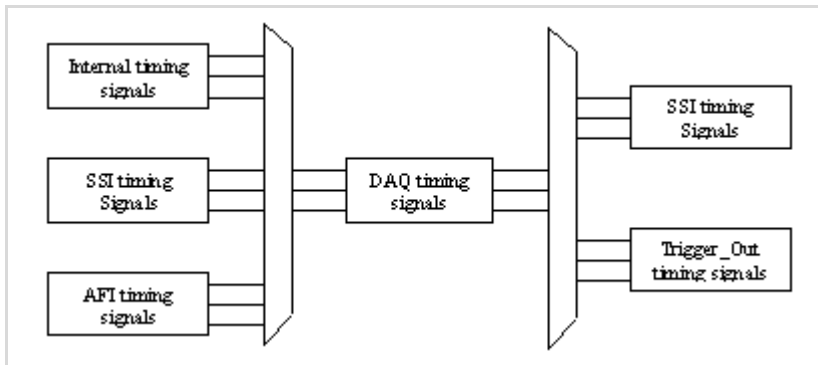


Figure 4-38: DAQ signals routing



You can utilize the flexible timing signals through our software drivers, then simply and correctly connect the signals with the PCI/PCIe/PXI-62204/62205/62206/62208 card. Here is the summary of the DAQ timing signals and the corresponding functionalities for PCI/PCIe/PXI-62204/62205/62206/62208 card.

Timing signal category	Corresponding functionality
SSI/PXI signals	Multiple cards synchronization
AFI signals	Control PCI/PCIe/PXI-62204/62205/62206/62208 by external timing signals

**Table 4-8: User-controllable Timing Signals and Functionalities**

## DAQ timing signals

---

**NOTES** Refer to section 4.1 for the internal timing signal definition.

The PCI/PCIe/PXI-62208 card supports SCAN\_START, ADCONV and DA\_TRIG, DAWR.

---

The user-controllable DAQ timing-signals contain:

1. TIMEBASE, providing TIMEBASE for all DAQ operations, which could be from internal 40 MHz oscillator, EXTTIMEBASE from I/O connector or the SSI\_TIMEBASE. Note that the frequency range of the EXTTIMEBASE is 1 MHz to 40 MHz, and the EXT-TIMEBASE must be TTL-compatible.
2. AD\_TRIG, the trigger signal for the A/D operation, which could come from external digital trigger, analog trigger, internal software trigger, and SSI\_AD\_TRIG. Refer to section 4.5 for detailed description.
3. SCAN\_START, the signal to start a scan, which would bring the following ADCONV signals for AD conversion, and could come from the internal SI\_counter, AFI[0] and SSI\_AD\_START. This signal is synchronous to the TIMEBASE. Note that the AFI[0] should be TTL-compatible and the minimum pulse width

should be the pulse width of the TIMEBASE to guarantee correct functionalities.

4. ADCONV, the conversion signal to initiate a single conversion, which could be derived from internal counter, AFI[0] or SSI\_ADCONV. Note that this signal is edge-sensitive. When using AFI[0] as the external ADCONV source, each rising edge of AFI[0] would bring an effective conversion signal. Also note that the AFI[0] signal should be TTL-compatible and the minimum pulse width is 20 ns.
5. DA\_TRIG, the trigger signal for the D/A operation, which could be derived from external digital trigger, analog trigger, internal software trigger, and SSI\_AD\_TRIG. Refer to section 4.5 for detailed description.
6. DAWR, the update signal to initiate a single D/A conversion, which could be derived from internal counter, AFI[1] or SSI\_DAWR. Note that this signal is edge-sensitive. When using AFI[1] as the external DAWR source, each rising edge of AFI[1] would bring an effective update signal. Also note that the AFI[1] signal should be TTL-compatible and the minimum pulse width is 20 ns.

## Auxiliary Function Inputs (AFI)

You can use the AFI in applications that take advantage of external circuitry to directly control the PCI/PCIe/PXI-62204/62205/62206/62208 card. The AFI includes two categories of timing signals: one group is the dedicated input, and the other is the multi-function input. Table 4-9 illustrates this categorization.

Category	Timing signal	Functionality	Constraints
Dedicated input	EXTTIMEBASE	Replace the internal TIMEBASE	<ul style="list-style-type: none"> <li>• TTL-compatible</li> <li>• 1 MHz to 40 MHz</li> <li>• Affects on both A/D and D/A operations.</li> </ul>
	EXTDTRIG	External digital trigger input for A/D operation	<ul style="list-style-type: none"> <li>• TTL-compatible</li> <li>• Minimum pulse width = 20ns</li> <li>• Rising edge or falling edge</li> </ul>
	EXTWFTRG	External digital trigger input for D/A operation	<ul style="list-style-type: none"> <li>• TTL-compatible</li> <li>• Minimum pulse width = 20ns</li> <li>• Rising edge or falling edge</li> </ul>
Multi-function input	AFI[0] (Dual-functions)	Replace the internal ADCONV	<ul style="list-style-type: none"> <li>• TTL-compatible</li> <li>• Minimum pulse width = 20ns</li> <li>• Rising-edge sensitive only</li> </ul>
		Replace the internal SCAN_START	<ul style="list-style-type: none"> <li>• TTL-compatible</li> <li>• Minimum Pulse width &gt; 2/TIMEBASE</li> </ul>
	AFI[1]	Replace the internal DAWR	<ul style="list-style-type: none"> <li>• TTL-compatible</li> <li>• Minimum pulse width = 20ns</li> <li>• Rising-edge sensitive only</li> </ul>

**Table 4-9: Auxiliary Function Input Signals and Functionalities**

### EXTDTRIG and EXTWFRIG

EXTDTRIG and EXTWFRIG are dedicated digital trigger input signals for A/D and D/A operations respectively. Refer to section 4.5 for details.

### EXTTIMEBASE

When the applications needs specific sampling frequency or update rate that the card could not generate from its internal TIMEBASE — the 40 MHz clock — you could utilize the EXTTIMEBASE with internal counters to achieve the specific timing intervals for both A/D and D/

A operations. Note that once you choose the TIMEBASE source, both A/D and D/A operations will be affected because A/D and D/A operations share the same TIMEBASE.

### **AFI[0]**

Alternatively, you can also directly apply an external A/D conversion signal to replace the internal ADCONV signal. This is another way to achieve customized sampling frequencies. The external ADCONV signal can only be inputted from the AFI[0]. As section 4.1 describes, the SI\_counter triggers the generation of the A/D conversion signal, ADCONV, but when using the AFI[0] to replace the internal ADCONV signal, the SI\_counter and the internally generated SCAN\_START is not effective. By controlling the ADCONV externally, you can sample the data according to external events. In this mode, the Trigger signal and trigger mode settings are not available.

AFI[0] could also be used as SCAN\_START signal for A/D operations. Refer to section 4.1 and section 4.6 for detailed descriptions of the SCAN\_START signal. When using external signal (AFI[0]) to replace the internal SCAN\_START signal, the pulse width of the AFI[0] must be greater than two time of the period of Timebase. This feature is suitable for the PCI-62200/PCIe-62200/PXI-62200 Series, which can scan multiple channels data controlled by an external event. Note that the AFI[0] is a multi-purpose input, and it can only be utilized for one function at any one time.

### **AFI[1]**

Regarding the D/A operations, users could directly input the external D/A update signal to replace the internal DAWR signal. This is another way to achieve customized D/A update rates. The external DAWR signal can only be inputted from the AFI[1]. Note that the AFI[1] is a multi-purpose input, and it can only be utilized for one function at any one time. AFI[1] currently only has one function. JYTEK reserves it for future development.

## **System Synchronization Interface**

SSI (System Synchronization Interface) provides the DAQ timing synchronization between multiple cards. In PCI/PCIe/PXI-62204/62205/62206/62208 card, we designed a bi-directional SSI I/O to provide flexible connection between cards and allow one SSI master to output the signal

and up to three slaves to receive the SSI signal. Note that the SSI signals are designed for card synchronization only and not for external devices.

SSI Timing Signal	Setting	Function
SSI_TIMEBASE	Master	Send the TIMEBASE out
	Slave	Accept the SSI_TIMEBASE to replace the internal TIMEBASE signal.
SSI_ADCONV	Master	Send the ADCONV out
	Slave	Accept the SSI_ADCONV to replace the internal ADCONV signal.
SSI_SCAN_START	Master	Send the SCAN_START out
	Slave	Accept the SSI_SCAN_START to replace the internal SCAN_START signal.
SSI_AD_TRIG	Master	Send the internal AD_TRIG out
	Slave	Accept the SSI_AD_TRIG as the digital trigger signal.
SSI_DAWR	Master	Send the DAWR out.
	Slave	Accept the SSI_DAWR to replace the internal DAWR signal.
SSI_DA_TRIG	Master	Send the DA_TRIG out.
	Slave	Accept the SSI_DA_TRIG as the digital trigger signal.

**Table 4-10: SSI Timing Signal and Functions**

In PCI form factor, there is a connector on the top right corner of the card for the SSI. Refer to section 2.3 for the connector position. All the SSI signals are routed to the 20-pin connector from the FPGA. To synchronize multiple cards, users can connect a special ribbon cable (ACL-SSI) to all the cards in a daisy-chain configuration.

In PXI form factor, we utilize the PXI trigger bus built on the PXI backplane to provide the necessary timing signal connections. All the SSI signals are routed to the P2 connector. No additional cable is needed. For detailed information of the PXI specifications, refer to the PXI Specification Revision 2.0 from PXI System Alliance ([www.pxisa.org](http://www.pxisa.org)).

The six internal timing signals could be routed to the SSI or the PXI trigger bus through software drivers. Refer to section 4.6 for detailed information on the six internal timing signals. Physically, the signal routings are accomplished in the FPGA. Cards that are connected together through the SSI or the PXI trigger bus, will still achieve synchronization on the six timing signals.

## The SSI/PXI Mechanism

We adopt master-slave configuration for SSI/PXI. In a system, for each timing signal, there shall be only one master, and other cards are SSI slaves or with SSI function disabled.

For each timing signal, the SSI master does not have to be in a single card. For example:

We want to synchronize the A/D operation through the ADCONV signal for four PCI/PCIe/PXI-62204/62205/62206/62208 cards. Card 1 is the master, and Card 2, 3, 4 are slaves. Card 1 receives an external digital trigger to start the post trigger mode acquisition. The SSI setting could be:

- ▶ Set the SSI\_ADCONV signal of Card 1 to be the master.
- ▶ Set the SSI\_ADCONV signals of Card 2, 3, 4 to be the slaves.
- ▶ Set external digital trigger for Card 1's A/D operation.
- ▶ Set the SI\_counter and the post scan counter (PSC) of all other cards.
- ▶ Start DMA operations for all cards, so all the cards are waiting for the trigger event.

When the digital trigger condition of Card 1 occurs, Card 1 will internally generate the ADCONV signal and output this ADCONV signal to SSI\_ADCONV signal of Card 2, 3 and 4 through the SSI/PXI connectors. Thus we can achieve 16-channel acquisition simultaneously.

You could arbitrarily choose each of the six timing signals as the SSI master from any one of the cards. The SSI master can output the internal timing signals to the SSI slaves. With the SSI, users could achieve better card-to-card synchronization.

Note that when power-up or reset, the DAQ timing signals are reset to use the internal generated timing signals.

## 5 Calibration

This chapter introduces the calibration process to minimize AD measurement errors and DA output errors.

### 5.1 Loading Calibration Constants

The PCI/PCIe/PXI-62204/62205/62206/62208 card is factory-calibrated before shipment. The associated calibration constants of the TrimDACs firmware to the onboard EEPROM. TrimDACs are devices containing multiple DACs within a single package. TrimDACs do not have memory capability. That means the calibration constants do not retain their values after the system power is turned off. Loading calibration constants is the process of loading the values of TrimDACs firmware stored in the onboard EEPROM. JYTEK provides a software utility that automatically reads the calibration constants automatically, if necessary.

There is a dedicated space for storing calibration constants in the EEPROM. In addition to the default bank of factory calibration constants, there is one user-utilization bank. This bank allows you to load the TrimDACs firmware values either from the original factory calibration or from a subsequently-performed calibration.

Because of the fact that measurements and outputs errors may vary depending on time and temperature, it is recommended that you calibrate the card when it is integrated in your computing environment. The auto-calibration function is presented in the following sections.



## 5.2 Auto-calibration

Through the PCI/PCIe/PXI-62204/62205/62206/62208 card auto-calibration feature, the calibration software measures and corrects almost all calibration errors without any external signal connections, reference voltage, or measurement devices.

The PCI/PCIe/PXI-62204/62205/62206/62208 card comes with an onboard calibration reference to ensure the accuracy of auto-calibration. The reference voltage is measured in the production line through a digital potentiometer and compensated in the software. The calibration constant is memorized after this measurement. We do not recommend adjustment of the onboard calibration reference except when an ultra-precision calibrator is available.

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### NOTES

- Warm the card up for at least 15 minutes before initiating auto-calibration.
  - Remove the cable before auto-calibrating the card since the DA outputs are changed during the process.
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## 5.3 Saving Calibration Constants

When auto-calibration is completed, you can save the new calibration constants to the user-configurable banks in the EEPROM. The date and the temperature when you ran auto-calibration is saved with the calibration constants. You can store three sets of calibration constants according to three different environments and re-load the calibration constants later.

## Warranty Policy

Thank you for choosing JYTEK. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. All JYTEK products come with a limited two-year warranty, one year for products bought in China:
  - ▶ The warranty period starts on the day the product is shipped from JYTEK's factory.
  - ▶ Peripherals and third-party products not manufactured by JYTEK will be covered by the original manufacturers' warranty.
  - ▶ For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. JYTEK is not responsible for any loss of data.
  - ▶ Please ensure the use of properly licensed software with our systems. JYTEK does not condone the use of pirated software and will not service systems using such software. JYTEK will not be held legally responsible for products shipped with unlicensed software installed by the user.
  - ▶ For general repairs, please do not include peripheral accessories. If peripherals need to be included, be certain to specify which items you sent on the RMA Request & Confirmation Form. JYTEK is not responsible for items not listed on the RMA Request & Confirmation Form.

2. Our repair service is not covered by JYTEK's guarantee in the following situations:
  - ▶ Damage caused by not following instructions in the User's Manual.
  - ▶ Damage caused by carelessness on the user's part during product transportation.
  - ▶ Damage caused by fire, earthquakes, floods, lightening, pollution, other acts of God, and/or incorrect usage of voltage transformers.
  - ▶ Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
  - ▶ Damage caused by leakage of battery fluid during or after change of batteries by customer/user.
  - ▶ Damage from improper repair by unauthorized JYTEK technicians.
  - ▶ Products with altered and/or damaged serial numbers are not entitled to our service.
  - ▶ This warranty is not transferable or extendible.
  - ▶ Other categories not protected under our warranty.
3. Customers are responsible for shipping costs to transport damaged products to our company or sales office.

If you have any further questions, please email our service center: [service@jytek.com](mailto:service@jytek.com).



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